1. Objective
The objective of this lab is to design and build the common-emitter amplifier with partial bypass of the emitter resistor to control the AC voltage gain.

2. Components

<table>
<thead>
<tr>
<th>Qty</th>
<th>Device</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2N2222 BJT Transistor</td>
</tr>
</tbody>
</table>

3. Introduction
One of the most popular single-transistor BJT amplifier designs is the common emitter (CE) amplifier design. The CE amplifier is relatively simple to bias, delivers a high voltage gain, and is easy to understand. In this lab, you will design and build such an amplifier. The procedure for this lab is straightforward. First, you will design a controlled gain amplifier for your prelab assignment. This process will involve designing the 4-resistor bias circuit and tailoring the frequency response of the amplifier circuit to meet the requirements. Hint: design for the Vout peak voltage and input resistance Rin. Then you will build the amplifier in the lab and test it to see whether it meets the requirements.

You should refer to your lab lecture notes, your Electronics II Lecture notes, your textbook, the course website, and other reference material to determine how best to design your amplifier. This lab is intended as a design project and not as a step-by-step guide.

Use BJT Design Section 2

4. Requirements
Your amplifier design must meet the following requirements.

<table>
<thead>
<tr>
<th>Requirement</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage Gain (Reb Bypassed)</td>
<td>$</td>
</tr>
<tr>
<td>Low Frequency Cutoff (FL)</td>
<td>Between 100 Hz and 300 Hz</td>
</tr>
<tr>
<td>High Frequency Cutoff (FH)</td>
<td>Between 50 kHz and 150 kHz</td>
</tr>
<tr>
<td>Input Impedance</td>
<td>Between 800Ω and 10KΩ</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>1.5V_p</td>
</tr>
<tr>
<td>Load Resistance</td>
<td>1.5 KΩ</td>
</tr>
<tr>
<td>Total Emitter Resistance</td>
<td>Two Resistors, $R_e = R_{ef} + R_{eb}$</td>
</tr>
<tr>
<td>Power Supply Voltage</td>
<td>12 V_{dc}</td>
</tr>
</tbody>
</table>

Table 1. Common-emitter amplifier requirements.

5. Prelab Design Project
You will design an amplifier in this prelab design project. The design will make use of a partially bypassed emitter resistor Reb, and an emitter bypass capacitor Ce, thus changing the gain and input impedance of the amplifier. The values of the capacitors will also change from design to design. Units must be included as well (it is permissible to include a table of final values for clarity if you would prefer, but again, all work must be handwritten and be shown clearly somewhere).
Use the following fixed component values in your circuit:

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_i$</td>
<td>$150,\Omega$</td>
</tr>
<tr>
<td>$C_{byp}$</td>
<td>choose a value</td>
</tr>
<tr>
<td></td>
<td>0.1µF</td>
</tr>
<tr>
<td></td>
<td>0.047µF</td>
</tr>
<tr>
<td></td>
<td>0.01µF</td>
</tr>
</tbody>
</table>

Table 2. Fixed component values.

5.1 DC Bias

**Begin by designing the Q-point** based on the output and input requirements. Use this to design the DC bias for the amplifier. The emitter resistor $R_e$ is the sum of the two emitter resistors $R_{em}$ unbypassed and $R_{em}$ bypassed emitter resister. The values of these resistors will control the Voltage Gain ($A_v$) of the amplifier. Note that the location and value of the capacitors do not affect the biasing, so the values you calculate here will be valid for the amplifier design. Once you have designed the DC bias, use the transistor characteristics for the 2N2222 transistor to determine the transistor parameters for where you are operating. Note that there is no single correct answer and that your design may differ significantly from your colleagues. You must show all your work and walk through all calculations.
Choose $V_E$ to be between 2V and 3V. $V_B = V_E + V_{BE}$

If you need to set the input impedance to a required value.

Set $R_{in} = R_{in} - R_i$

$R_{in2} = R_b1 || R_b2 || \left[ r_\pi + (\beta + 1)\left(\frac{R_f}{\left(\frac{R_{in1}}{R_{in2}}\right)}\right)\right]$  

CE with Ref

$V_B = V_{cc}\frac{R_b2}{R_b1 + R_b2}$.  

Solve for $R_b1$, and $R_b2$

<table>
<thead>
<tr>
<th>Component Values</th>
<th>Amplifier Parameters</th>
<th>Voltages and Currents</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{b1}$</td>
<td>Beta DC From curve</td>
<td>$V_{ce}$</td>
</tr>
<tr>
<td>$R_{b2}$</td>
<td>Beta AC From curve</td>
<td>$V_{be}$</td>
</tr>
<tr>
<td>$R_c$</td>
<td>$r_\pi$</td>
<td>$V_e$</td>
</tr>
<tr>
<td>$R_f$</td>
<td>$r_o$ From curve</td>
<td>$I_b$</td>
</tr>
</tbody>
</table>

Table 3. DC Bias and Amplifier Parameters

5.2 AC: Design

We will now design and calculate the ac characteristics for the partially bypassed CE amplifier, with the emitter capacitor, partially Ref is not bypassed and Reb is bypassed. Table 4 shows all of the values you need to calculate. Be sure to show all work. You may use equations given in the lab lecture, class lecture, or from a textbook. Be sure you understand how to use the equations, though—if assumptions are included, you must state these and show that you meet them.

**For the FL low frequency cut off.**

We will set all 3 break points (n=3) to the same frequency this causes band spreading so FL = Fcin + Fcout + Fce will be incorrect. We will use a break point frequency for each capacitor of FL'.

$$FL' = FL \times \sqrt{2^{\frac{1}{n}}} - 1$$  

For each capacitor (Cin, Cout, Ce) use C=1 / (2 π FL' Req)

Where Req the equivalent resistance seen by the capacitor.

$$BW_{shrinkage} = \sqrt{2^{\frac{2}{n}}} - 1$$  

Where (n = 3) is the number of low frequency zeros at the same frequency.

$FL = \frac{(Fcin + Fcout + Fce)}{(BW_{shrinkage}\times n)}$ if all 3 break points (n=3) at the same frequency Fcin = Fcout = Fce = $FL \times BW_{shrinkage}$

**For the FH High frequency cut off.**

$$BW_{shrinkage} = \sqrt{2^{\frac{2}{n}}} - 1$$  

Where (n = 2) is the number of high frequency poles at the same frequency. $FH' = FH / (BW_{shrinkage})$

Chi, and Chi2 control the high frequency cutoff and will help prevent high frequency oscillations.

$$FH' = \frac{FH}{\sqrt{2^{\frac{2}{n}}} - 1}$$  

Where (n = 2) is the number of high frequency poles at the same frequency.

Chi, Chi2 = 1/(2 π FH' Req). Where Req the equivalent resistance seen by each capacitor.
5.3 AC: Gain of a Partial Emitter Bypass CE amp
Capacitor $C_e$ only bypassing $Reb$ and $Re = Ref + Reb$. The gain will be lower than if we bypassed both $Ref$ and $Reb$.

\[
A_{v2} = -\frac{\beta R_{L'}}{\frac{1}{r_n} + (\beta + 1)R_{ef}} \quad \text{Where and } R_{L'} = R_c||R_L
\]

<table>
<thead>
<tr>
<th>Component Values</th>
<th>Amplifier Parameters</th>
<th>Voltages, Currents, and Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{in}$</td>
<td>Voltage Gain</td>
<td>$V_{in}$</td>
</tr>
<tr>
<td>$C_{out}$</td>
<td>Current Gain</td>
<td>$V_{out}$</td>
</tr>
<tr>
<td>$C_e$</td>
<td>Power Gain (in dB)</td>
<td>$i_{in}$</td>
</tr>
<tr>
<td>$C_{hi}$</td>
<td>Low Frequency Cutoff</td>
<td>$i_{out}$</td>
</tr>
<tr>
<td></td>
<td>High Frequency Cutoff</td>
<td>$P_{in}$</td>
</tr>
<tr>
<td></td>
<td>Input Resistance</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Output Resistance</td>
<td>$P_{out}$</td>
</tr>
</tbody>
</table>

Table 4. Small Signal (ac) Amplifier Parameters

5.4 Computer-aided Analysis (25 Points)
Once you have completed your amplifier design, use a circuit simulator LTspice to analyze their performance. Note: Must include LTspice schematics. Generate the following plots for the amplifier design:

(a) A time-domain plot of the input and output, with the output voltage of 1.5$V_{pk}$ or greater at 5 kHz. The output should not have any distortion or clipping. Calculate the midband gain and indicate it on the plot. Compare this to your calculated values.

(b) An FFT of your time-domain waveform. Circle and indicate the height of any strong harmonics, in dB relative to your fundamental frequency at 5 kHz.

(c) A frequency sweep of the amplifier from 10 Hz to 1 MHz Indicate the high and low frequencies cutoffs on the plot (these should correspond to the half-power, or 3dB below midband ). Compare these to your calculated values.

5.5 Prelab Question
How could you vary the gain of the amplifier by using a potentiometer of a value equal to sum of $R_{ef}$, and $Reb$ without affecting the Q point? Draw a circuit.
6. Lab Procedure

6.1 Construct the CE amplifier shown in Figure 2. Must bypass the power supply on your proto board with a 0.1μF, 0.047μF or 0.001μF capacitor to prevent oscillations. Remember that $R_{gen}$ is internal to the function generator and is not in your circuit. Remember to use the two emitter resistors values from design. Record the values of the bias network resistors and the capacitors you used in the circuit.

6.2 Measure the following values: Measure at maximum undistorted output
   (a) Q-point: $V_c$, $V_b$, $V_e$, $V_{ce}$, $V_{be}$, $I_e$, and $I_c$.
   (b) Voltage, current, and power gains.
   (c) Maximum undistorted peak-to-peak output voltage measured at 5kHz.
   (d) Input and output resistance measured at 5kHz. Note use $R_i$ to calculate $I_{in}$.
   (e) Low and high cutoff frequencies (half power point).

Recall that input impedance is given by $R_{in} = V_{in}/I_{in}$, output impedance is given by $R_{out} = (V_{oc} - V_{out})/I_{Load}$, voltage gain is given by $A_v = V_{out}/V_{in}$, and current gain is given by $A_i = I_{load}/I_{in}$.

Additionally, plot the following: 4 plots
   (a) Input and output waveform at the maximum undistorted value.
   (b) FFT showing the fundamental and first few harmonics. Must add a power spectrum step to signal express scope capture.
   (c) Frequency response from 10 Hz to 1 MHz (set the input voltage to a value that does not cause distortion across the entire passband of the amplifier).

6.3 Replace the load resistor, $R_L$, with a 100 Ohm and a 10k resistor, and measure the maximum output swing and voltage gain without clipping. Comment on the loading effect, and remember to change back to a 1.5k load resistor after this step.
ECE 3274
Common Emitter Amplifier Lab
Data Sheet

Name: ______________________ Lab Date: ____________ Bench: ____________
Partner: ____________________ CRN: ________________

Remember to include units for all answers and to label all printouts. There are a total of 4 plots in this lab. Only one set of printouts is required per group. **10 point reduction** if you do not replace all connectors, components, and cables.

6.1 Component Values Measure before building.

\[ R_{b1}: \quad R_{b2}: \quad R_c: \quad \]
\[ R_{ef}: \quad R_{eb}: \quad R_L: \quad \]

6.2 Common-emitter amplifier. There are 4 plots at maximum undistorted output (Vin, Vout, Power spectrum, and AC sweep). \( I_B = I_E - I_C \).

**Capacitor Values:**

\[ C_{in}: \quad C_{out}: \quad \]
\[ C_e: \quad C_{hi}: \quad \]

**Q-Point (DC):**

\[ V_C: \quad V_B: \quad V_E: \quad \]

Calculate \( I_B: \quad I_C: \quad I_E: \quad \)

\[ V_{CE}: \quad V_{BE}: \quad V_{CC}: \quad \]

**Gain (AC):**

\[ \frac{\text{Voltage}}{\text{Current}}: \quad \frac{\text{Voltage}}{\text{Current}}: \quad \frac{\text{Voltage}}{\text{Current}}: \quad \text{Power:} \quad \]

**Voltage Output:**

\[ \text{Max:} \quad \]

**Resistance (AC):**

\[ \text{Input:} \quad \text{Output:} \quad \]

**Frequency Cutoff:**

\[ \text{Low:} \quad \text{High:} \quad \]

6.3 Common-emitter amplifier with a different load resistors find the maximum undistorted output (no plots).

100Ω Resistor:

\[ \text{Gain:} \quad \frac{\text{Voltage}}{\text{Current}}: \quad \frac{\text{Voltage}}{\text{Current}}: \quad \text{Power:} \quad \]

\[ \text{Voltage Output Vpp:} \quad \text{Max:} \quad \]

10kΩ Resistor:

\[ \text{Gain:} \quad \frac{\text{Voltage}}{\text{Current}}: \quad \frac{\text{Voltage}}{\text{Current}}: \quad \text{Power:} \quad \]

\[ \text{Voltage Output Vpp:} \quad \text{Max:} \quad \]

**Change** \( R_L = 1.5k \)