Project 3 – Digital Applications of the Operational Amplifier

Objective: This project will show the versatile operation of an operational amplifier in a voltage comparator (Schmitt trigger) circuit and a sample and hold circuit.

Components: 741 op-amp, 2N7000 MOSFET

Introduction:

A voltage comparator is a two-input circuit that compares the voltage at one input to the voltage at the other input. Usually one input is a reference voltage and the other input a time varying signal. If the time varying input is below or above the reference voltage, then the comparator provides a low or high output accordingly. The ideal operation of a comparator is shown in Figure 3-1. If V_{REF} is zero, the comparator can be used as a zero-crossing detector. If V_{REF} is not zero, the comparator can be referred to as a level detector. The comparator is the basis for most A/D circuits. In these A/D circuits, the reference voltage is gradually changed by a counter and compared to the analog input voltage until it equals the analog input voltage.

The Schmitt trigger is a comparator that uses hysteresis. The transfer characteristic of the Schmitt trigger is shown in Figure 3-2. The Schmitt trigger basically has two thresholds, one on each side of the reference voltage. This gives a buffer zone for the rejection of noise and interference of the input signal. The hysteresis enables the comparator to turn on at one voltage value and possibly turn off at another voltage value. For example, a decreasing signal will remain at Out+ until V_{TL} is crossed and then remain at Out- until the signal increases and crosses V_{TH}. If the noise voltage is a noisy input signal does not exceed the hysteresis voltage, then false, or multiple triggering is avoided. Hysteresis in the Schmitt trigger also ensures that the output is the same frequency as the input for noisy input signals that may cross the threshold several times while rising and falling. The Schmitt trigger is especially useful for slowly varying and noisy input signals. The operational amplifier in the comparator circuit of Figure 3-3 allows for flexibility in setting the gain, thresholds, and reference voltage.

For an analog signal to be processed by a digital system it must be converted to a digital signal. A sample and hold circuit is one way of accomplishing this conversion. In a sample and hold circuit, the analog input signal is sampled and then held at the same value until a new sample is taken. Two important properties of a sample and hold circuit are the highest possible sampling rate and how constant the sample remains during the hold interval.

The sample and hold circuit shown in Figure 3-4 uses an op-amp in the noninverting configuration and a MOSFET. The square wave input represents the sampling rate and the length of time to hold the sample. The MOSFET acts as a switch, which is on during sampling and off during the hold time. When the square wave is positive, the circuit samples the input signal. During sampling the MOSFET turns on to

complete the path to the capacitor and the circuit output is approximately the same as the input signal. When the square wave is negative, the circuit is in the hold mode. During the hold time the MOSFET turns off and the output is the value the capacitor charged to during the previous sampling interval.

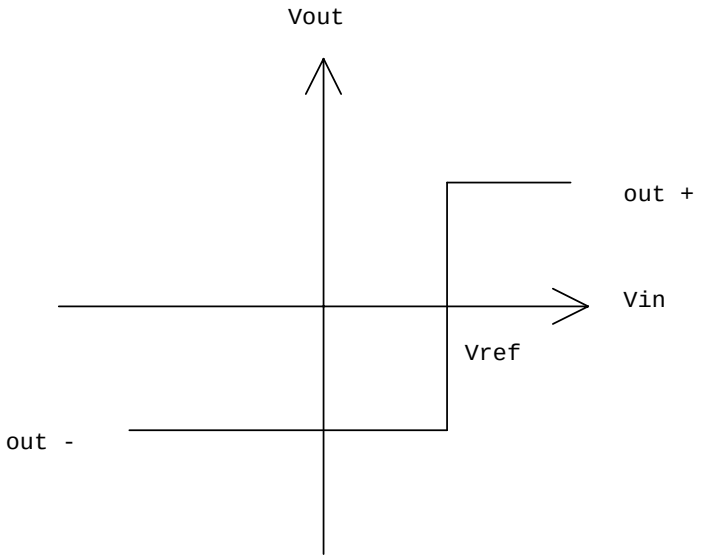


Figure 3 - 1: Ideal Comparator Transfer Characteristic

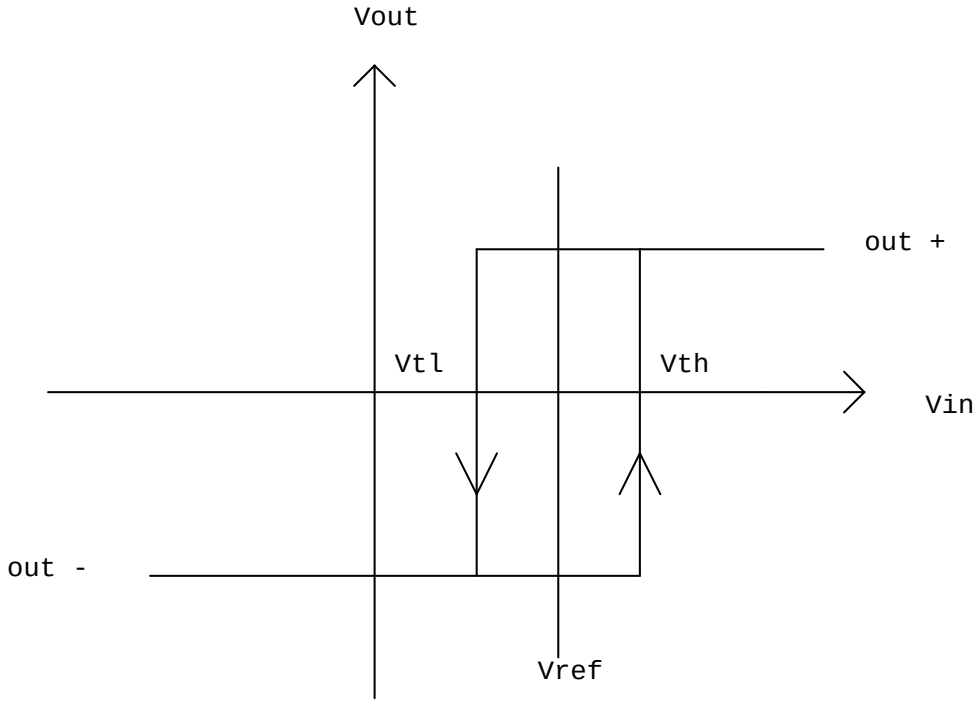
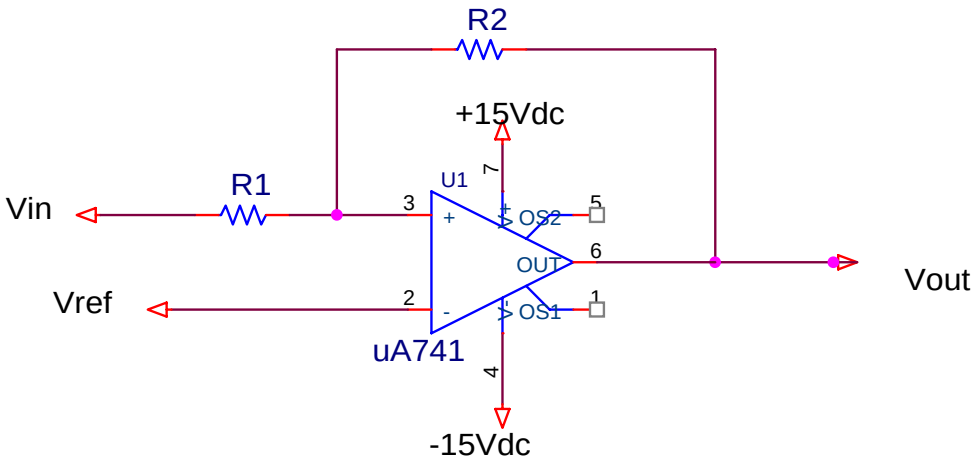


Figure 3 – 2: Comparator Transfer Characteristic with Hysteresis



Comparator with Hysteresis

Figure 3 – 3: Comparator with Hysteresis

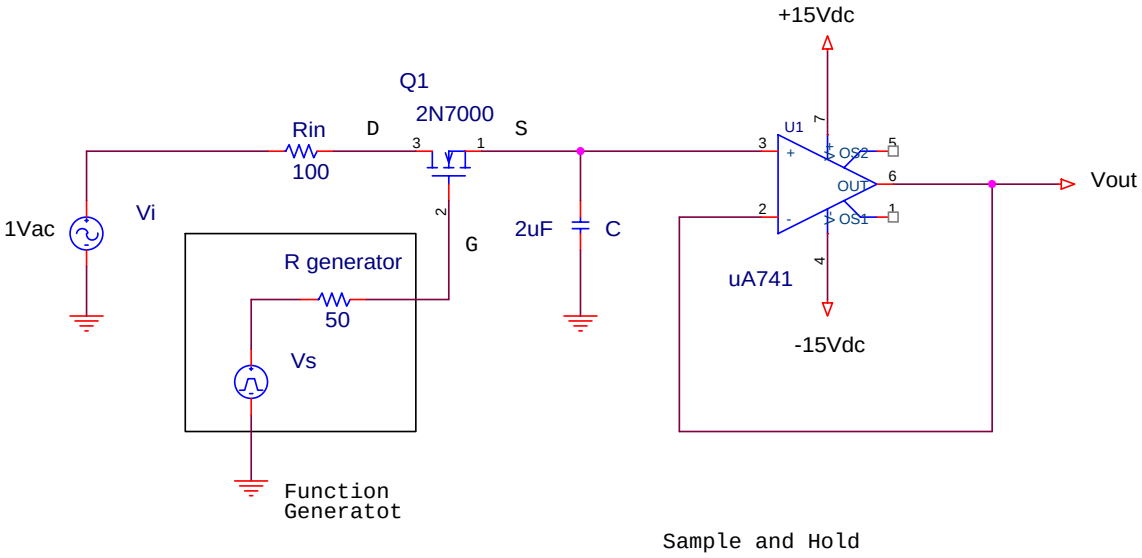


Figure 3 – 4: Sample and Hold

Design and prelab: Show all work, include schematics and calculations.

1. Find the relationship between the resistances in the comparator circuit and the thresholds V_{TL}, V_{TH} and V_{OUT} remember V_{TL} and V_{TH} are input voltages. Let Vref = 0. **Show all work**.

2. Modify the above equations for a reference voltage not equal to zero

3. Design a comparator circuit of Fig 3 – 3 such that the V_{TL} = -1V, V_{TH} = +1V, and V_{REF} = 0.0 V. Verify the comparator design with PSPICE. Sweep the DC input voltage: case one from –5V to +5V and, case two from +5V to –5V.

4. Verify the operation of the sample and hold circuit of Figure 3-4 with PSPICE®. Use Time Domain analysis to plot the waveform. Use an IRF150 for the MOSFET. Use a 1 V peak sine wave at 60 Hz for the input waveform. Use a 1kHz $20V_{pp}$ square wave as the gate input. Use ±15 V supplies for the op-amp.

Lab Procedure:

1. Construct the comparator circuit of Figure 3-3. Set the reference voltage to zero and the thresholds 1 V above and below zero. Use ±15V supplies for the op-amp.

2. Verify the comparator's operation by using computer control of the DC power supply to sweep the input voltage from –5V dc to +5 dc. Need to use two supplies in series, one to offset -5Vdc the other will sweep from 0Vdc to +10Vdc. Observe V_{TH} the high threshold voltage. Capture this graph,

3. Sweep the input voltage from +5V dc to –5V dc by sweeping the supply from +10Vdc to 0Vdc and observe V_{TL} the low threshold voltage. Capture this graph.

4. Now use a 2 V peak sine wave at 1 KHz as the input. Monitor the input and output waveforms on the oscilloscope. Measure the slope of the line between the low to high output limits and the high to low output limits. Capture this waveform, use this waveform to find the slew rate.

5. Construct the sample and hold circuit of Figure 3-4. Use a square wave with an upper limit of +10V and a lower limit of –10 V for V_s to drive the gate of the MOSFET. To begin with, use R_1=100 Ω and C = 2 μF, and a sampling rate around 1 kHz. Use ±15 V supplies for the op-amp.

6. Use the Variac with the step-down transformer for the input waveform. With the transformer plugged into the Variac, adjust the Variac until the secondary voltage from the transformer has a peak of ~ 1V.

7. Capture the input and output waveforms on the oscilloscope trigger on the input. Do the two waveforms match? Note any offset error.

Questions:

1. How can you determine the maximum frequency at which the Schmitt trigger can operate from the slew rate data collected? What is the maximum frequency using the slew rate specification?

2. For the sample and hold circuit, determine the approximate decay rate of the capacitor voltage in mV/s during the hold mode for the data. Calculate the decay rate by using the input bias current from the data sheet of 80nA to find the decay rate.

3. What is the maximum hold time for the sample and hold circuit if the capacitor voltage cannot change by more than 10%? Assume initial capacitor voltage is 1 V.

Report Project 3 Digital Application of the Operational Amplifier.

Name:_____ Date:_____ Lab Bench#_____

Remember to include all of your prelab assignment.

Answer the questions at the end of the lab procedure and turn in with the report.

1. Values of components from the design of the comparator with hysteresis.

   R_1= _____ R_2 = _____

   Include schematics drawing.

   Values of components use to build the comparator with hysteresis.

   R_1= _____ R_2 = _____

2. High threshold V_{TH}=_____V_{DC}
   Print the DC sweep.

3. Low threshold V_{TL}=_____V_{DC}
   Print the DC Sweep.

4. Calculate from the oscilloscope display.
   Slew rate from low to high. =_____
   Slew rate from high to low = _____
   Maximum frequency calculated =_____
   Print oscilloscope waveform.

5. Include schematics drawing.

7. Delay time from input to output.=_____
   Change in amplitude from input to output. =_____
   Decay rate during the hold time. =_____
   Do the waveforms match?

   Note any offset errors in time or amplitude?

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Answer the questions at the end of the lab procedure and turn in with the report.