

TTL LOGIC and RING OSCILLATOR TTL

We will examine two digital logic inverters. The first will have a passive resistor pull-up output stage. The second will have an active transistor and current limit resistor output stage.

The third circuit will use an odd number of integrated circuit (IC) inverters connected in a loop to produce a free running oscillation frequency based on the time delay of the inverters.

PreLab: Single transistor Inverter Part 1

PART 1. Build in LTspice a TTL logic inverter with $V_{cc} = 5V_{dc}$. $R_{load} = 1k\Omega$

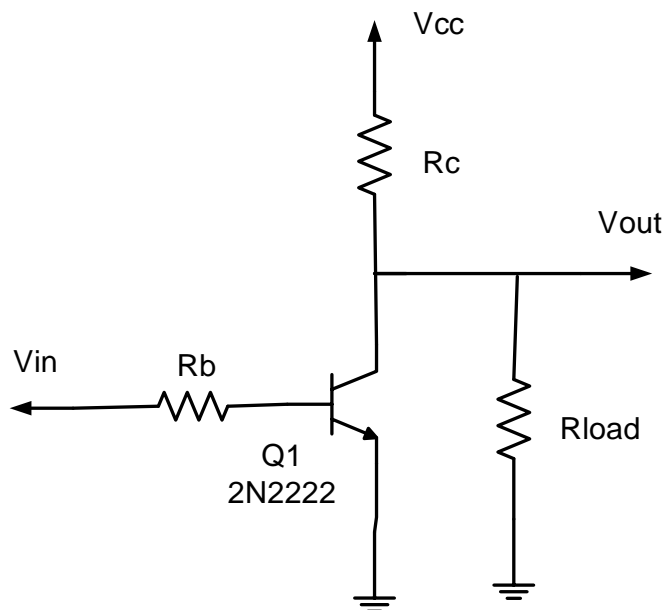
A1. Set $V_{in} = 5V$ so that the output is Low. Now run a Bias Point simulation (.OP) on the circuit.

What is the output current through the load? What is the output voltage?

A2. Set $V_{in} = 0V$ so that the output is High. Now run a Bias Point simulation (.OP) on the circuit.

What is the output current through the load? What is the output voltage?

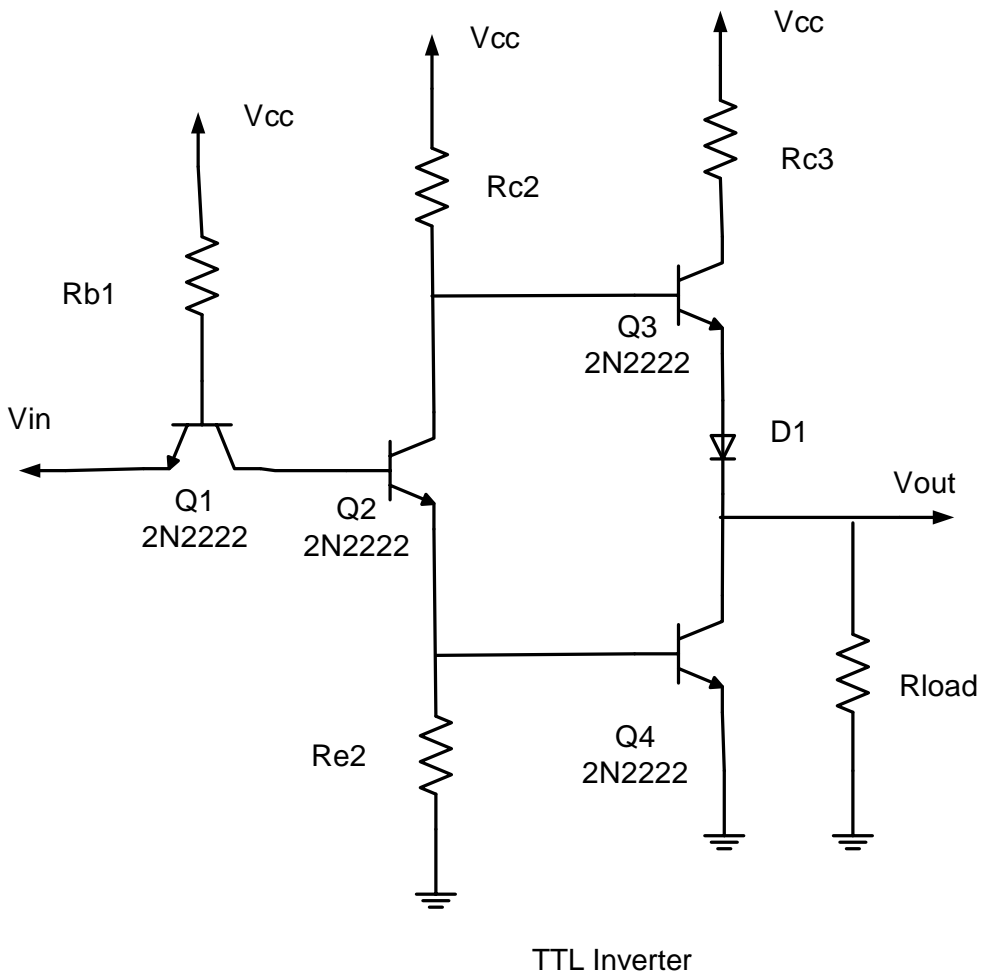
B1. Run a DC sweep from 0V to 5V on the input V_{in} while observing the change in the output V_{out} . What input voltage does the inverter switch at measured at the 50% of difference between V_{out} Max and V_{out} Min point?



Single transistor inverter

$V_{cc} = 5V_{dc}$. $R_{load} = 1k\Omega$ $R_b = 1k\Omega$, $R_c = 2.2k\Omega$

PreLab: TTL Inverter Part 2



$V_{cc} = 5V_{dc}$

$R_{b1} = 3.9k$, $R_{c2} = 1.5k$, $R_{e2} = 1k$, $R_{c3} = 120$, $R_{load} = 1k$ and, $D1 = 1N4148$

Part 2: TTL inverter

A1. Change $V_{in} = 5V$ so that the output is low. Now run the .OP simulation on the circuit. $R_{load} = 1k\Omega$. What is the output current through the load? What is the output voltage?

A2. Change $V_{in} = 0V$ so that the output is High. Now run the .OP simulation on the circuit. $R_{load} = 1k\Omega$. What is the output current through the load? What is the output voltage?

A3. Now change the Rload to 47K Ω . Run the .OP simulation on the circuit. Observe the output current through the load. Run A1, and A2 again. What changes do you notice in the current? What changes do you notice in the output voltage?

B1. Run a DC sweep from 0V to 5V on the input Vin while observing the change in the output Vout. What input voltage does the TTL inverter switch at measured at the 50% of difference between Vout Max and Vout Min point?

Prelab: Ring Oscillator Part 3

Go to the web and get a copy of a data sheet for a TTL 74LS04 hex inverter. What is the propagation delay of a single inverter section?

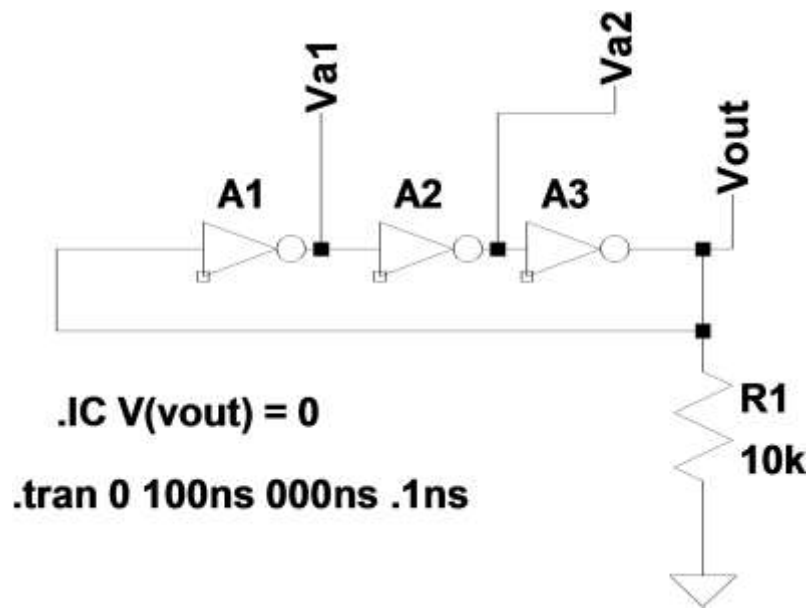
Setup each inverter parameters:

Low voltage level Vlow = 0.2, High voltage level Vhigh = 4.0,

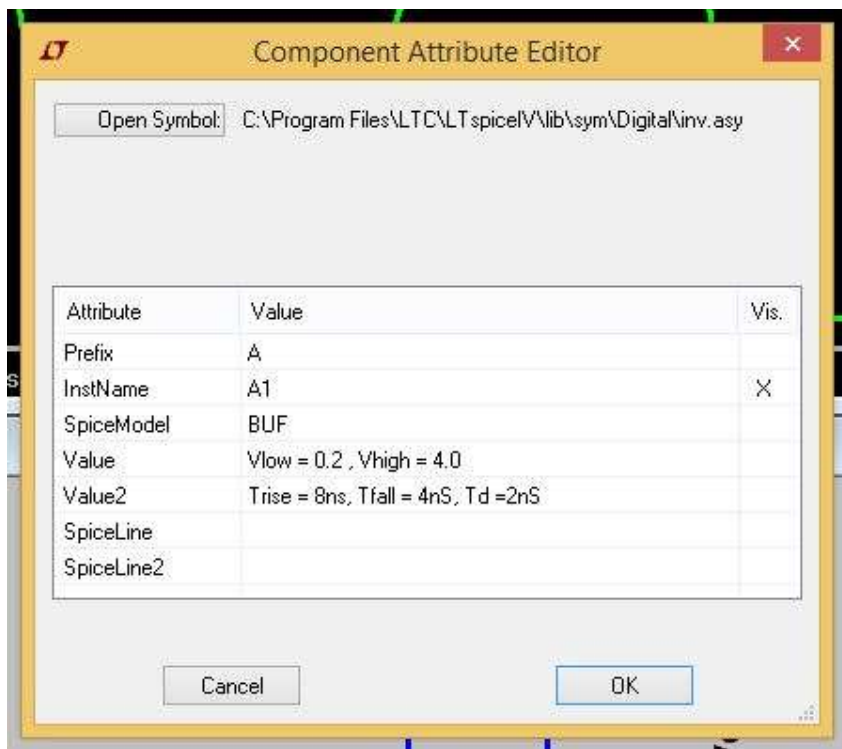
Rise time Trise = 8nS, Fall time Tfall = 4nS, Delay time Td = 2nS.

Add an initial condition Spice directive. IC V(vout) = 0 on the schematic.

Build the inverter Ring Oscillator shown below in LTspice use a generic inverter (inv) under. LTspice > components > digital > inv. Select the transient simulation from 0nS to 100nS Timestep 0.1nS, and uncheck Start external DC supply voltages at 0V, and uncheck skip initial operating point solution. Graph the output waveform and label your graph to be turned in. What is the amplitude and frequency?



LTspice Ring oscillator



Required Attachments: (8 total)

DC Sweep of inverter and list of .OP voltage and currents (3 attachments)

TTL logic inverter schematic with list of .OP voltages and currents of $1k\Omega$ (2 attachments)

TTL logic inverter schematic with list of .OP voltages and currents of $47K\Omega$ (2 attachment)

Waveform output of ring oscillator: Remember to uncheck box "Skip initial operating Point solution". (1 attachment)

Lab Exercise

Experiment TTL

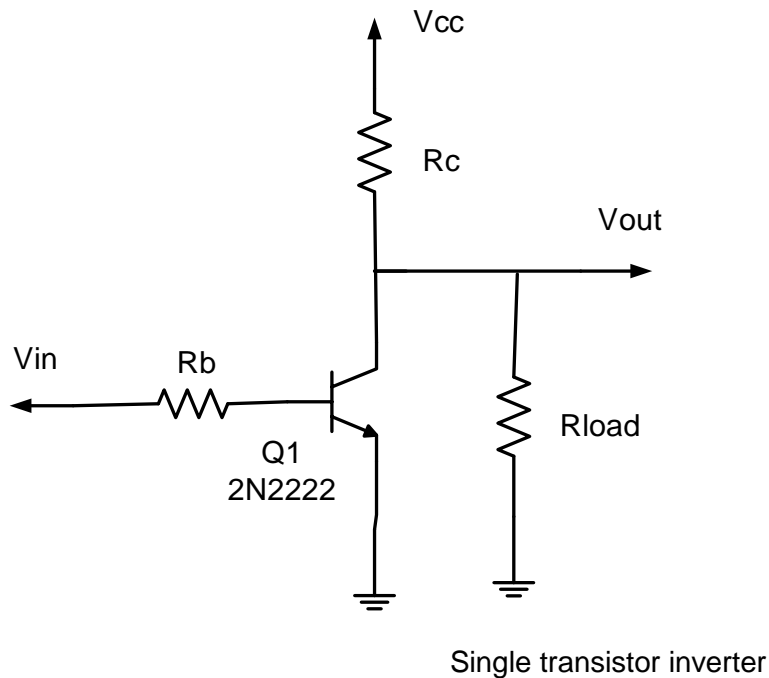
TTL Logic and Ring Oscillator

1. Build the single transistor inverter circuit with $V_{cc} = 5V_{dc}$.

Perform a DC sweep: sweep V_{in} from 0V to 5V step size = 100mV on V_{in} .

A. Capture and save the output voltage (V_{out}) of the circuit with $R_{load} = 1K\Omega$.

B. Repeat with $R_{load} = 47K\Omega$



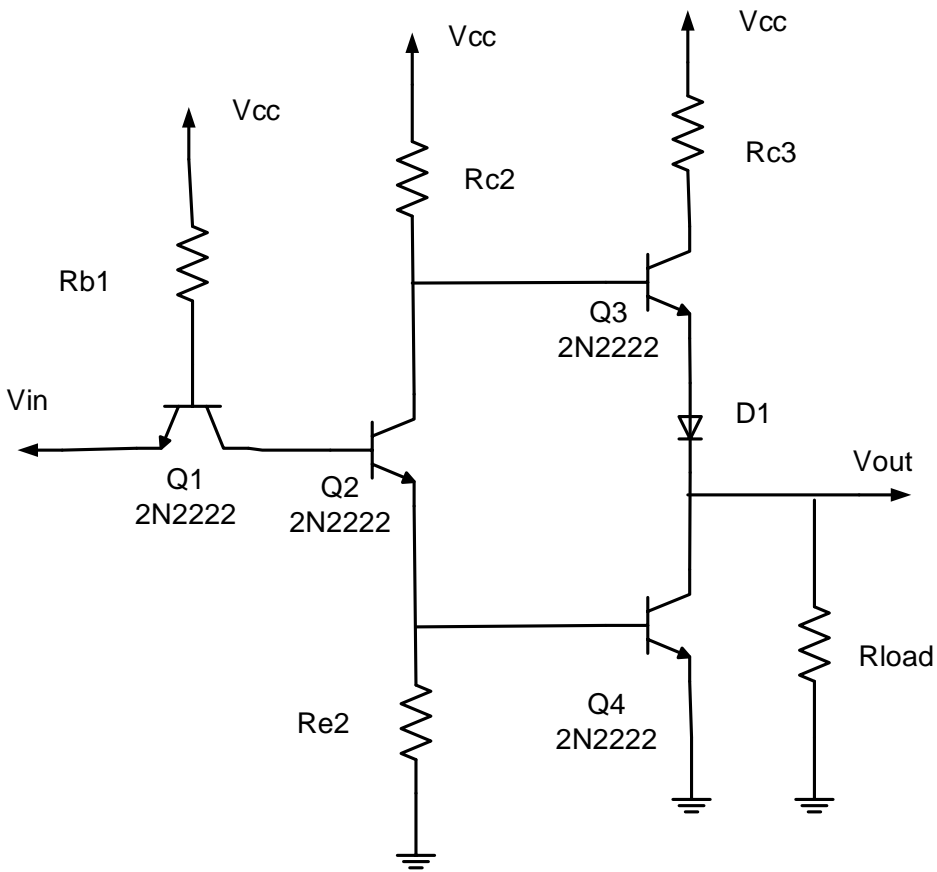
$V_{cc} = 5\text{Vdc}$, $R_b = 1\text{k}\Omega$, $R_c = 2.2\text{k}\Omega$, $R_{load} = 1\text{k}\Omega$, or $R_{load} = 47\text{k}\Omega$

2. Build the **TTL inverter** circuit with $V_{cc} = 5\text{Vdc}$.

Perform a DC sweep: sweep V_{in} from 0V to 5V step size = 100mV on V_{in} .

A. Capture and save the output voltage V_{out} of the circuit with $R_{load} = 1\text{k}\Omega$.

B. Repeat with $R_{load} = 47\text{k}\Omega$.



TTL Inverter

$V_{cc} = 5V_{dc}$

$R_{b1} = 3.9k$, $R_{c2} = 1.5k$, $R_{e2} = 1k$, $R_{c3} = 120$, $R_{load} = 1k$ and, $D1 = 1N4148$

Compare the two output voltage graphs. At what input voltage level do you notice that the output makes the transition from logic 1 (high) to logic 0 (low) for the three inverters?

Transition Voltage = V_{in} when $V_{out} = 50\%$ of the ($V_{out\ max} - V_{out\ min}$) where V_{out} transitions from High to Low

Compare the 4 output voltage graphs. When the output is in the logic 1 (high) state, what differences in maximum voltage level do you notice for the two inverters circuits?

3. Build the inverter **Ring Oscillator** shown in your pre-lab. Use 2 10X scope probe to observe the oscillator output (pin 6) on the oscilloscope (**2 to 5 complete cycles**) Time base = 20nS / Div. The 10X probe will help to reduce capacitance in the input cable. Save this waveform.

Vcc = 5v Pin 14, Ground on Pin 7.

What is the output frequency of the Ring Oscillator? How does this measured frequency compare with the LTspice frequency?

Use the measured frequency to determine the propagation delay of the inverters in 74LS04 inverter chip. How does the measured propagation delay compare with the data sheet spec? Remember there are 3 inverters. Divide the period by the number of propagation delays in the ring oscillator.

TTL LOGIC and RING OSCILLATOR Data Sheet

Name: _____ Name: _____ Date: _____

Bench # _____ Instructor: _____ Class time, day: _____

Compare the Transition Voltages for the two inverters. Transition Voltage = V_{in} when $V_{out} = 50\%$ of ($V_{out\ max}$) when V_{out} transitions from High to Low

1. Single transistor inverter

DC sweep of V_{out} , $R_{load} = 1K$ include plot

Input Transition Voltage: _____ Max output Voltage: _____

DC Sweep of V_{out} , $R_{load} = 47k$ **include plot**

Input Transition Voltage: _____ Max output Voltage: _____

2. TTL inverter

DC sweep plot V_{out} , $R_{load} = 1K$ include plot

Input Transition Voltage: _____ Max output Voltage: _____

DC Sweep plot V_{out} , $R_{load} = 47k$ **include plot**

Input Transition Voltage: _____ Max output Voltage: _____

3. Ring Oscillator

5. Frequency measured in lab _____ Frequency from LTspice _____

6. Measured propagation delay per inverter _____

Stated propagation delay range from data sheet per inverter _____

Required Attachments: (5 Total)

Output of Single transistor inverter (2 plots). R_{load} of 1K and 47k.

Output of TTL Inverter (2 plots). R_{load} of 1K and 47k.

Scope capture of ring oscillator output V_{out} (2 to 5 complete cycles) set time to 200nS