ECE 2274

TTL LOGIC and RING OSCILLATOR TTL

We will examine two digital logic inverters. The first will have a passive resistor pull-up output stage. The second will have an active transistor and current limit resister output stage.

The third circuit will use an odd number of integrated circuit (IC) inverters connected in a loop to produce a free running oscillation frequency based on the time delay of the inverters.

PreLab: Single transistor Inverter Part 1

A. Build in LTspice a TTL logic inverter with $V_{cc} = 5\text{Vdc}$. $R_{load} = 1\,\text{k}\Omega$

Set $V_{in} = 5\text{V}$ so that the output is Low. Now run a Bias Point simulation on the circuit.

$V_{cc} = 5\text{Vdc}$. $R_{load} = 1\,\text{k}\Omega$ $R_{b} = 1\,\text{k}\Omega$, $R_{c} = 2.2\,\text{k}\Omega$

What is the output current through the load? What is the output voltage?

Run a DC sweep from 0V to 5V on the input $V_{in}$ while observing the change in the output $V_{out}$. 
PreLab: TTL Inverter Part 2

Vcc = 5Vdc

Rb1 = 3.9k, Rc2 = 1.5k, Re2 = 1k, Rc3 = 120, Rload = 1k and, D1 = 1N4148

A. Change Vin = 0V so that the output is high. Now run a Bias Point simulation on the circuit. Rload = 1kΩ. What is the output current through the load? What is the output voltage?

B. Now change the Rload to 47KΩ. Run the same Bias Point simulation on the circuit. Observe the output current through the load. What changes do you notice in the current? What changes do you notice in the output voltage?
Prelab: Ring Oscillator Part 3

Go to the web and get a copy of a data sheet for a TTL 74LS04 hex inverter. What is the propagation delay of a single inverter section?

Setup each inverter parameters:
- Low voltage level $V_{low} = 0.2$, High voltage level $V_{high} = 4.0$,
- Rise time $T_{rise} = 8\text{nS}$, Fall time $T_{fall} = 4\text{nS}$, Delay time $T_d = 2\text{nS}$.

Add an initial condition Spice directive. IC $V(vout) = 0$ on the schematic.

Build the inverter Ring Oscillator shown below in LTspice use a generic inverter. Select the transient simulation from $0\text{nS}$ to $100\text{nS}$ Timestep $0.1\text{nS}$, and uncheck Start external DC supply voltages at $0V$, and uncheck skip initial operating point solution. Graph the output waveform and label your graph to be turned in. What is the amplitude and frequency?

\[ .IC \ V(vout) = 0 \]
\[ .tran 0 \ 100\text{ns} \ 000\text{ns} \ .1\text{ns} \]
Required Attachments:

DC Sweep of inverter

TTL logic inverter schematic with voltages and currents of 1kΩ

TTL logic inverter schematic with voltages and currents of 47K Ω

Output of ring oscillator: Remember to skip initial bias point
Lab Exercise

Experiment TTL

TTL Logic and Ring Oscillator

1. Build the single transistor inverter circuit with Vcc = 5Vdc.

Perform a DC sweep: sweep Vin from 0V to 5V step size = 100mV on Vin.

A. Capture and save the output voltage (Vout) of the circuit with Rload = 1KΩ.

B. Repeat with Rload = 47KΩ

\[ Vcc = 5Vdc, \quad Rb = 1k\Omega, \quad Rc = 2.2k\Omega, \quad Rload = 1k\Omega, \text{ or } Rload = 47k\Omega \]
2. Build the TTL inverter circuit with Vcc = 5Vdc.

Perform a DC sweep: sweep Vin from 0V to 5V step size = 100mV on Vin.

A. Capture and save the output voltage Vout of the circuit with Rload = 1KΩ.
B. Repeat with Rload = 47KΩ.

\[
\begin{align*}
Vcc &= 5Vdc \\
Rb1 &= 3.9k, Rc2 = 1.5k, Re2 = 1k, Rc3 = 120, Rload = 1k \text{ and, } D1 = 1N4148
\end{align*}
\]
Compare the two output voltage graphs. At what input voltage level do you notice that the output makes the transition from logic 1 (high) to logic 0 (low) for the three inverters?

Transition Voltage = \( V_{in} \) when \( V_{out} = 50\% \) of \( (V_{out} \text{ max}) \) where \( V_{out} \) transitions from High to Low

Compare the 4 output voltage graphs. When the output is in the logic 1 (high) state, what differences in maximum voltage level do you notice for the two inverters circuits?

3. Build the inverter Ring Oscillator shown in your pre-lab. Use the 10X scope probe to observe the oscillator output (pin 6) on the oscilloscope (2 to 5 complete cycles). The 10X probe will help to reduce capacitance in the input cable. Save this waveform.

\[ V_{cc} = 5\text{v Pin 14, Ground on Pin 7}. \]

What is the output frequency of the Ring Oscillator? How does this measured frequency compare with the LTspice frequency?

Use the measured frequency to determine the propagation delay of the inverters in 74LS04 inverter chip. How does the measured propagation delay compare with the data sheet spec? Remember there are 3 inverters. Divide the period by the number of propagation delays in the ring oscillator.
Compare the Transition Voltages for the two inverters. Transition Voltage = Vin when Vout= 50% of (Vout max) when Vout transitions from High to Low

1. **Single transistor inverter**

   DC sweep plot Vout, Rload = 1K include plot
   
   Input Transition Voltage: _________ Max Voltage: _________
   
   DC Sweep plot Vout, Rload = 47k include plot
   
   Input Transition Voltage: _________ Max Voltage: _________

2. **TTL inverter**

   DC sweep plot Vout, Rload = 1K include plot
   
   Input Transition Voltage: _________ Max Voltage: _________
   
   DC Sweep plot Vout, Rload = 47k include plot
   
   Input Transition Voltage: _________ Max Voltage: _________

3. **Ring Oscillator**

   5. Frequency measured in lab__________ Frequency from LTspice__________
   
   6. Measured propagation delay per inverter________________________
   
      Stated propagation delay range from data sheet per inverter__________

   **Required Attachments:**

   Output of Single transistor inverter (2 plots).
   
   Output of TTL Inverter (2 plots).
   
   Scope capture of ring oscillator output (2 to 5 complete cycles)