EXPERIMENT ***Power Factor Correction***

Power Factor Correction Requirements

OBJECTIVE

The objective of this module is to enhance the importance of power factor correction (PFC) by exploring some concepts related to standards, total harmonic distortion (THD) and PFC circuits.

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BACKGROUND INFORMATION

As predicted by the Electric Power Research Institute (EPRI), more than 60% of utility power will be processed through some form of power electronics equipment by the year 2010. However, most of that equipment generates pulsating currents to the utility grids with poor power quality and high harmonic contents that adversely affect other users.

The situation has drawn the attention of regulatory bodies around the world. Governments are tightening regulations, setting new specifications for low harmonic current, and restricting the amount of electro-magnetic waves that can be emitted.

Through this module, the student will become familiar with the importance of PFC in electronic equipment by exploring some concepts related to standards, THD and PFC circuits.

Definitions

The power factor (PF) is defined as the ratio between the average power (averaged in a line period) and the product of the rms values of the input voltage and current; that is,

$$PF = \frac{average\,power}{apparent\,power} \equiv \frac{\frac{1}{T}\int_0^T v(t)\,i(t)\,dt}{\sqrt{\frac{1}{T}\int_0^T v(t)^2\,dt}\sqrt{\frac{1}{T}\int_0^T i(t)^2\,dt}}, \quad (1)$$

where *v(t)* and *i(t)* are, respectively, the input voltage and current waveforms and T is the line period.

The THD is defined as

$$THD \equiv \frac{\sqrt{\sum_{n=2}^{\infty} I_n{}^2}}{I_1}, \quad (2)$$

where I_n and I_1 are the amplitudes of the *n*th harmonic component and of the fundamental component, respectively, of the line current *i(t)*. The relationship between PF and THD can be determined by defining the distortion factor as follows:

$$\frac{PF}{DPF} \equiv \sqrt{\frac{1}{1+(THD)^2}}, \quad (3)$$

where *DPF* is the displacement factor, which is equal to the well-known "cosine of ϕ" when the line voltage is sinusoidal, ϕ being the angle by which the fundamental component of *i(t)* lags *v(t)*.

This relationship is plotted in Figure 1. The distortion factor of a waveform with a moderate amount of distortion is quite close to the unity. For example, if the waveform contains a third harmonic whose magnitude is 10% of the fundamental, the distortion factor is 99.5%. Increasing

the third harmonic to 20% decreases the distortion factor to 98%, and a 33% harmonic magnitude yields a distortion factor of 95%. So the PF is not significantly degraded by the presence of harmonics unless the harmonics are quite large in magnitude.

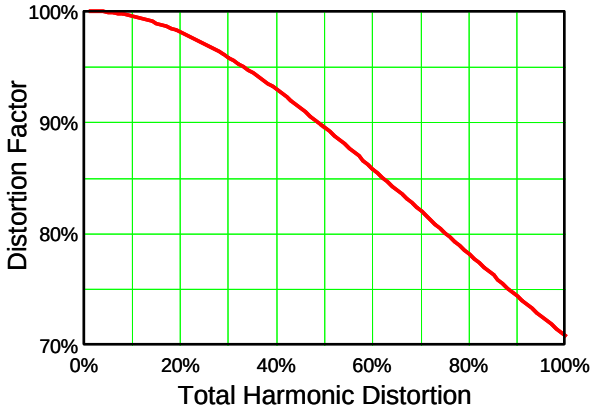
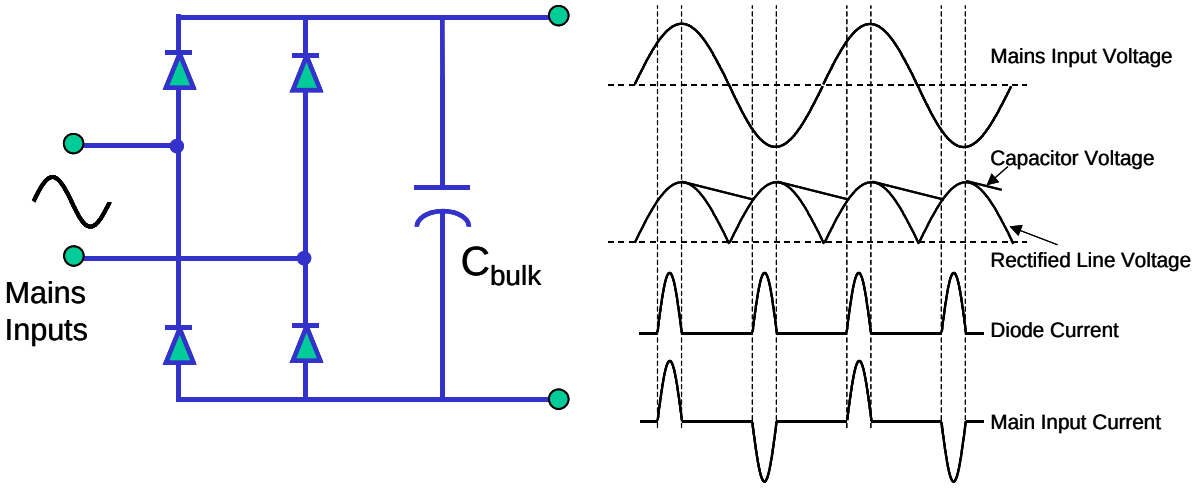


Figure 1. Relationship between total harmonic distortion and distortion factor.

The Off-Line Rectifier

The conventional input stage of an off-line switching power supply design is shown in Figure 2(a). It is comprised of a full-bridge rectifier followed by a large-input-filter capacitor. This input-filter capacitor reduces the ripple on the voltage waveforms into the DC converter stage. The problem with this input circuit is that it produces excessive peak input currents and high harmonic distortion on the line. The high distortion in the input current occurs due to the fact that the diode rectifiers only conduct during a short interval. This interval corresponds to the time when the mains instantaneous voltage is greater than the capacitor voltage. Since the capacitor must meet hold-up time requirements (during fault conditions, the mains are disconnected from the circuit for some cycles) its time constant is much grater than the frequency of the mains. Therefore, the mains instantaneous voltage is greater than the capacitor voltage only for very short periods of time, during which, the capacitor must be charged fully. Therefore, large pulses of current are drawn from the line over a very short period of time, as shown in Figure 2(b). This is true for all rectified AC sinusoidal signals with capacitive filtering; they draw high amplitude current pulses, the fundamental current of the line current is essentially in phase with the voltage, and the displacement factor is close to the unity. However, the low-order current harmonics are quite large, close to that of the fundamental. A typical current spectrum is shown in Figure 3. The THD for this kind of rectification is usually in the range 55% to 65%. The resulting PF is similar in value.



(a) (b)

Figure 2. (a) Typical input stage for an off-line switching power supply and (b) main waveforms.

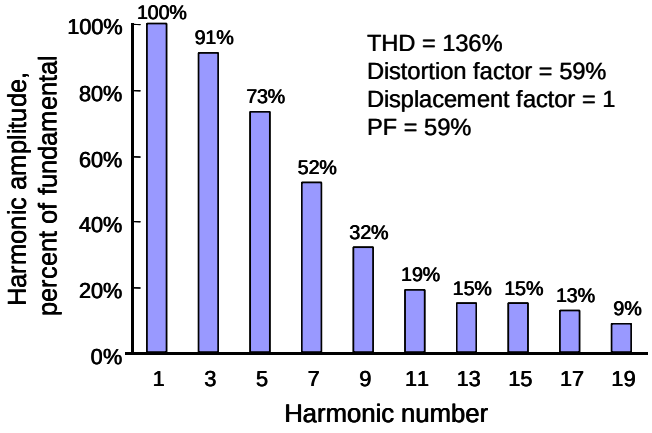


Figure 3. Typical AC line current spectrum for the input stage of an off-line switching power supply.

However, as can be seen, this system has many disadvantages:

- It creates harmonics and electromagnetic interference (EMI).
- It produces high losses.
- It requires over-dimensioning of parts.
- It reduces maximum power capability from the line.

Conventional AC rectification is thus a very inefficient process, resulting in high electricity cost for the utility company and waveform distortion of the current drawn from the mains. It produces a large spectrum of harmonic signals that may interfere with other equipment. A circuit similar to that shown in Figure 2(a) is used in most mains-powered conventional and switch mode power supplies. At higher power levels (200 to 500 watts and higher) severe interference with other electronic equipment may become apparent due to these extra harmonics reflected back into the power utility line. Another problem is that the power utility line cabling, the installation, and the transformer must all be designed to withstand these peak current values.

Problems of Low Power Factor and High Harmonic Distortion

This section briefly presents some of the problems related to low PF and high harmonic distortion.

Less Useful Power Available

The power utility line circuit is designed, rated and fused based on the amount of current that it can safely deliver. Since low PF increases the apparent current from the source, the amount of useful power that can be drawn from the circuit is lowered due to thermal limitation. We will use as an example the 120V 15A outlet circuit commonly found in offices and homes in the United States. If we assume that the overall efficiency of the power conversion system inside the equipment is 80% and that the line current is derated by 20% to avoid nuisance tripping, then the useful power available from such a circuit, assuming a unity power factor (best possible case), can be calculated as:

$$Po_{max} = 120V \times (15A \times 0.80) \times 0.80 = 1152 \text{ watts.}$$

Repeating the calculation using the uncorrected PF of 0.59 that we calculated in the previous section, we obtain the maximum available useful power to be:

$$Po_{max} = 120V \times (15A \times 0.80) \times 0.59 \times 0.80 = 680 \text{ watts.}$$

Note the enormous decrease in available load power. The low PF could have been caused by either a phase-shift (displacement) or harmonic distortion with an equally devastating impact on the level of useful power.

AC Distributed Cost

Low PF increases not only the apparent line current but also the additional current capacity cost money. This starts within the equipment itself and extends all the way back to the generation and distribution systems of the electric utility. Wire sizes within the equipment and the building must be increased to carry the additional current. When there is an abundance of loads with poor PF, this need for increased capacity will require additional power generation and distribution capability. This cost increase will, to a first approximation, be directly proportional to the inverse of the PF:

$$Cost\,of\ additional\ power\,capability = \frac{1}{power\ factor}.$$

Thus, if all connected loads had a PF of 0.59 rather than 1, the increase in the hardware cost for supplying the additional current would be approximately 69%. The power losses in any dissipative circuit elements (such as wire connections and transformer windings) will be proportional to square of the apparent current. Therefore, cost associated with providing this dissipated power will also scale inversely with the PF. Utility meters in residential and office environments will actually only register the real power drawn from the power utility line, so that the user is not directly penalized in terms of utility costs for the reactive components of the power.

Voltage Waveform Distortion

For the purpose of simplicity, most of the calculations have assumed that the AC source impedance is zero and the AC voltage waveform is not distorted by nonlinear current waveforms. In reality, the source impedance, while low, is not zero. For fault protection purposes, the conductor sizes get smaller as the AC power gets closer to the final load electronics. The smallest conductors are within the equipment itself, and high level of distortion on the current waveform will start to affect the quality of the voltage waveform, making it non-sinusoidal. If this voltage distortion becomes severe, it can cause operational problems with the power supply and with other nearby equipment connected to the same power source.

EMC

The higher line current associated with poor PF, especially if distortion and higher-frequency harmonics are present, can make for a much more difficult electromagnetic compatibility (EMC) environment. Passive PFC solutions often entail adding a capacitor, which often also acts as an

EMC filter to reduce noise imposed onto the power utility line. Active PFC approaches can be a source of additional switching activity and associated EMC. However, this noise is high frequency in nature and can be controlled by filters utilizing physically small components, often at only one location in the power system.

Three-Phase System

While we are focusing our attention on single-phase systems, the problem of harmonic distortion in some three-phase systems should be mentioned. Specifically, a four-wire three-phase system containing a neutral conductor can be severely compromised by harmonic current content on its load. Loads that are not balanced from phase to phase will result in undesired neutral current content. But even in the best case of completely balanced loads, harmonic contents in the loads will appear in the neutral conductor. The good news is that most of the harmonics (including the fundamental) will cancel out and will not result in a net current in the neutral conductor. The bad news is that the so-called "triple" harmonics (3^{rd}, 6^{th}, 9^{th}….) will appear and be directly accumulative in the neutral conductor. For example, if the three loads each only contained a 3^{rd} harmonic that was 15% of the fundamental, the neutral would experience a 3^{rd} harmonic current equal to 45% of the fundamental current. Since the neutral conductors are sized according to the assumption that they will conduct minimal current, this will create a significant problem for the power system.

Regulatory Non-Compliance

Because of the problems cited above, all industrialized countries have established regulations and standards that address PF and harmonic distortion on their power utilities; these will be addressed in the next section. Without compliance to the appropriate standard(s), the off-line power supply with conventional input rectifier will have a difficult time gaining acceptance in the market. In fact, it may be illegal to attempt to sell it. These legal' and profit-related issues make it mandatory that power system designers understand the PF and current distortion potential of their designs and also appropriate methods for making them compliant.

PFC techniques are being increasingly used in new off-line power converter designs. This is motivated both by the concerns listed above and by regulatory requirements, and is overall a positive development for equipment users and the power utilities. Most PFC circuits are now active rather than passive, and while this results in exceptional PFC performance, it requires that

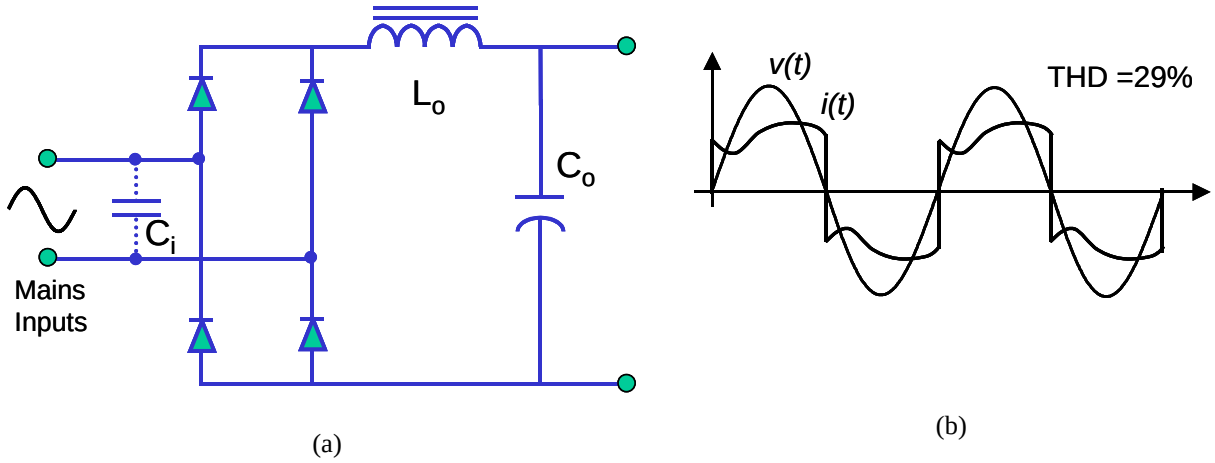
additional circuitry be added. The added circuitry can have the following negative impacts on the system:

- Additional cost and complexity for the power converter
- Lower power converter reliability
- Slightly lower efficiency (additional conversion stage sometimes needed)

In spite of these potential limitations, including active PFC is most often a very good design tradeoff for the power system. The above concerns are usually more than offset by the reduced input current, undistorted current waveforms, and additional useful power capability of converters that utilize PFC.

Active PFC

Improvements in the PF and harmonic distortion can be achieved by modifying the input stage of the off-line converter shown in Figure 2. Passive solutions (as shown in Figure 4) can be used to achieve this objective for low-power applications. With a large DC filter inductor, the single-phase full-wave rectifier produces a square wave line current waveform, attaining a PF of 90% and 48% THD. With smaller values of inductance, these achievements are degraded. However, the large size and weight of these elements, in addition to their inability to achieve unity PF and null THD, render them unacceptable in many applications.



(a) (b)

Figure 4. (a) Circuit diagram of full-wave rectifier with LC filter, and (b) typical waveforms.

Active solutions are a more suitable option for improving PF and harmonic distortion in higher-power applications. In these active solutions, a converter with switching frequencies higher than the AC line frequency is placed between the output of the diode rectifiers and the bulk capacitor, as shown in Figure 5. The reactive elements of this converter are small, because the size depends on the converter switching frequency rather than the AC line frequency. The function of this converter is to behave as an ideal resistive load for the output of the diode rectifiers in order to eliminate the generation of line current harmonics. Due to this characteristic, the converter is also known as a *resistor emulator*.

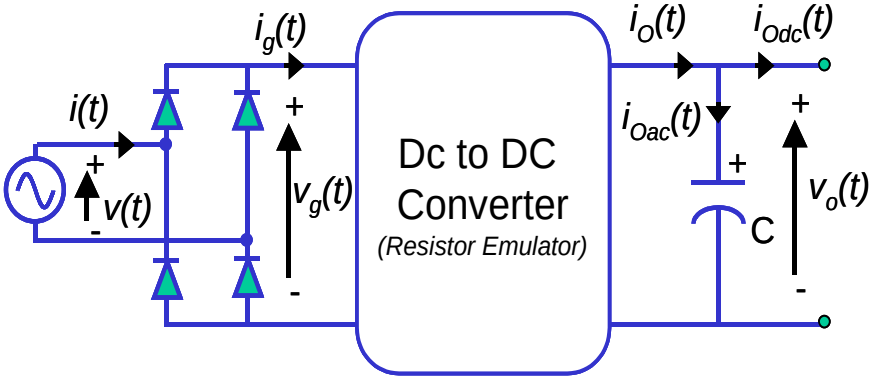


Figure 5. Circuit diagram of an active power factor correction scheme.

Now let explore the characteristics that this converter should offer in order to be used as a resistor emulator. First, we can express the sinusoidal input voltage as a function of the peak input voltage as follows:

$$v(t) = V_g \sin(wt), \tag{4}$$

where w is 2π times the AC line frequency. Since the diode rectifiers see the resistor emulator as a resistance, the rectifier input current should be proportional to the rectifier input voltage, such that

$$i_g(t) = \frac{v_g(t)}{R_e}, \tag{5}$$

where R_e is the hypothetical value of this resistor. In this condition, each pair of diagonal diode rectifiers conducts 180° of the AC line period. Therefore, $v_g(t)$ will be a rectified sinusoidal waveform and can be expressed as follows:

$$v_g(t) = V_g \left|\sin(wt)\right|. \tag{6}$$

Since the current $i_g(t)$ at the output of the rectifier is related to the voltage $v_g(t)$ by Equation (5), it can be concluded that the current $i_g(t)$ will also be a sinusoidal rectifier, and can be expressed as follows:

$$i_g(t) = \frac{V_g \left|\sin(wt)\right|}{R_e} = I_g \left|\sin(wt)\right|, \tag{7}$$

where I_g is the peak value of the current $i_g(t)$. Under this condition, the input current $i(t)$ will also be purely sinusoidal:

$$i(t) = I_g \sin(wt). \tag{8}$$

Considering that $v(t)$ and $i(t)$ are two sinusoidal waveforms in phase, the PF will be unity with null harmonic distortion.

It is important to consider some important statements related to the characteristics of the resistor emulator. First, the resistor emulator is a switching converter; therefore, in ideal conditions it does not present power dissipation. Second, the switching frequency (typically 50 to 200 kHz) is much higher than the AC line frequency (50 or 60 Hz). That means that the concept of quasi-static

conditions can be applied for the analysis of the converter. This concept considers that the input voltage does not change during a switching cycle of the resistor emulator.

In addition, as mentioned before, the reactive elements are selected according to the switching frequency. Therefore, they can only store energy during a switching cycle and not during a long period of time as this one presented during a line cycle.

After defining the previous consideration, the instantaneous power in the input of the resistor emulator is defined as:

$$p(t) = v_g(t)\, i_g(t) = V_g\, I_g \sin^2(wt)\,. \tag{9}$$

This instantaneous input power should be equal to the output power of the *resistor emulator*. From Figure 5, we can determine the value of this output power as follows:

$$p_O(t) = i_O(t)\, v_O(t)\,. \tag{10}$$

It is important to mention that the instantaneous input power of the resistor emulator is pulsating with a frequency equal to twice the AC line frequency. Since the final objective is to generate a continuous bus voltage, an additional component should be included to allow the bus voltage to become constant. This component is the capacitor C in Figure 5. Assuming that the value of this capacitor is big enough to consider that the bus voltage is constant ($v_O(t)$ = V_O= constant) and having power balance in the resistor emulator, we have:

$$i_O(t) = \frac{V_g\, I_g}{V_O} \sin^2(wt)\,. \tag{11}$$

This equation can be also expressed as:

$$i_O(t) = \frac{V_g\, I_g}{2V_O} - \frac{V_g\, I_g}{2V_O} \cos(2wt)\,, \tag{12}$$

where we have the following DC component:

$$i_{Odc}(t) = \frac{V_g\, I_g}{2V_O}\,, \tag{13}$$

which flows through the DC bus, and the following AC component:

$$i_{Odc}(t) = \frac{V_g I_g}{2V_O}\cos(2wt), \tag{14}$$

which flows entirely through the capacitor C considering that the value of this capacitor was well designed. Figure 6 shows the waveforms for $v_g(t)$, $i_g(t)$ and $i_O(t)$. It is important to point out that during the period of time for which $i_O(t)$ is bigger that $i_{Odc}(t)$ (therefore $i_{Oac}(t)$ is positive), the capacitor C is charged. In the rest of the time, when $i_O(t)$ is less than $i_{Odc}(t)$ (therefore $i_{Oac}(t)$ is negative), the capacitor is discharged.

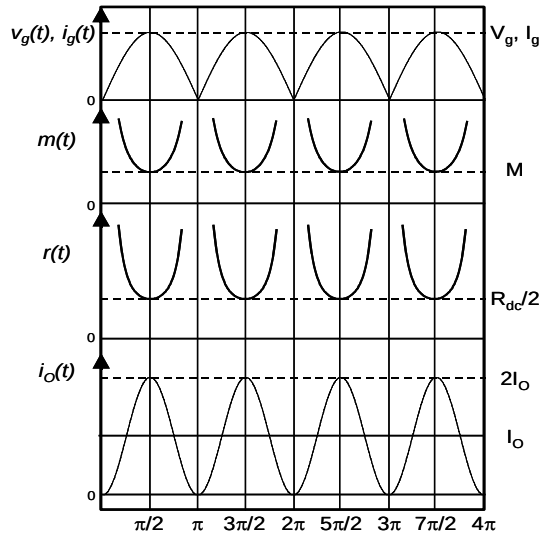


Figure 6. Main waveforms in a resistor emulator.

In addition, we can define the new term R_{dc} as the relationship between the voltage and current in the DC bus:

$$R_{dc} = \frac{V_O}{i_{dc}} \tag{15}$$

The term i_{dc} can be eliminated by using Equations (14) and (15) as follows:

$$\frac{V_g I_g}{V_O} = \frac{2V_O}{R_{dc}}. \tag{16}$$

In this way, we can express Equation (11) as follows:

$$i_O(t) = \frac{2V_O}{R_{dc}}\sin^2(wt). \tag{17}$$

Now, if we define the resistor seen by the resistor emulator, *r(t)* as the relationship between the voltage V_O in the output and the current $i_O(t)$, we obtain the following expression:

$$r(t) = \frac{V_O}{i_O(t)} = \frac{R_{dc}}{2\sin^2(wt)}. \quad (18)$$

From this equation we can make the first important statement related to the characteristics of the resistor emulator: It sees at the output a load resistor, which is different from the load resistor seen by the DC bus. Both load resistors are related by Equation (18); in this way the resistor emulator sees wide variations of load, with a range between $R_{dc}/2$ to an infinite value.

On the other hand, there is another important characteristic that should be present in the resistor emulator. By considering the converter conversion ratio, *m(t)* defined by the relationship between the constant output voltage V_O and $v_g(t)$, and using Equation (6), we can define the following expression:

$$m(t) = \frac{V_O}{v_g(t)} = \frac{M}{\sin(wt)}, \quad (19)$$

where $M=V_O/V_g$ is the relationship between the output voltage and the peak value of the AC line waveform. From Equation (19) we can state that the conversion ratio for a resistor emulator varies between infinity (at the AC line voltage zero crossing) and some minimum value *M* (at the peak of the AC line voltage waveforms).

Equations (18) and (19) are very important for defining the operating characteristics of a resistor emulator, and thus to select the DC/DC converter that can meet these requirements. Several pulse width modulation (PWM) topologies for DC/DC converters can be used as resistor emulators in a PF system. However, we will focus on the boost topology since it is the most popular implementation for medium- and high-power applications.

A system based on the continuous conduction mode (CCM) boost converter is shown in Figure 7. Ideally, the boost converter can produce any conversion ratio between one and infinity. Hence, the boost converter is capable of producing the *m(t)* given by Equation (19), provided that $V_o \geq V_g$. For a universal input voltage (90-240 V_{rms}), in order for the converter to achieve PFC, it should be designed so that the output voltage V_o is greater than the peak of the input line voltage. Assuming a maximum line voltage of 240 V_{rms} and allowing at least a 10% margin, a nominal V_o results in

380 V. The relative high output voltage is actually an advantage for the step-down converter following the CCM boost converter. The current levels in the silicon and transformer of the step-down converter are moderate, resulting in lower-cost devices. Another characteristic of the boost converter is that it can produce very low THD, with better transistor utilization than other approaches; the efficiency of the active boost circuit is very high, approaching 95%.

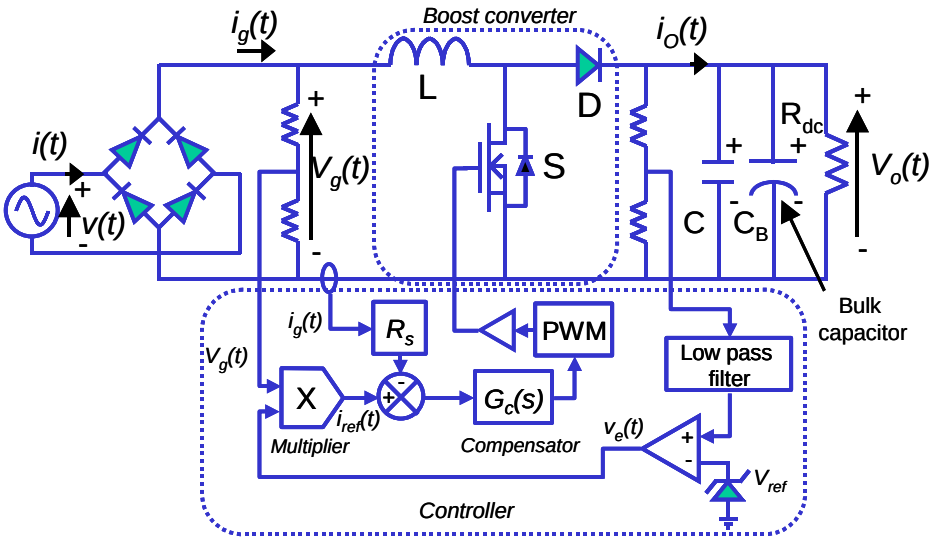


Figure 7. Rectifier system based on the boost converter using a multiplier controller.

The CCM boost converter needs two control loops to control both the input current and the output voltage. One of the control loops, the input current loop, commands the DC/DC converter to work as a half-sinusoidal current sink at its input. The other control loop, the output voltage loop, commands the DC/DC converter to work as a DC voltage source at its output. This kind of controller is typically called a multiplier controller. The basic simplified multiplier controller can be also seen in Figure 7. As shown, there is a feedback current loop that forces the pulse modulation of switch S in such a way that the input current follows the reference $i_{ref}(t)$. An analog multiplier creates $i_{ref}(t)$ by multiplying the rectified line voltage by the output of the voltage of the error amplifier $v_e(t)$. Thus, the input current is a rectified sinusoidal, the value of which depends on $v_e(t)$. In this way, $v_e(t)$ controls the power drawn from the utility line, and considering that the resistor emulator (in this case the boost converter) is a non-dissipative element, it also controls the power delivered to the load. It is equivalent to say that for every load, $v_e(t)$ determines the voltage that is applied to the load. Therefore, using a feedback loop of the output voltage whose output will be the error signal $v_e(t)$, the output voltage becomes perfectly constant.

It is important to point out that $v_e(t)$ must be constant; otherwise, the rectified input current would not be a rectified sinusoidal and neither would the utility line current. In order to meet the requirement for $v_e(t)$, a low-pass filter must be used to eliminate the ripple in the output voltage. This low-pass filter results in a slow feedback loop.

On the other hand, the current feedback loop should be as fast as possible to guarantee that the input current follows the reference $i_{ref}(t)$. For the implementation of the current feedback loop, either peak current mode control or average current mode control may be used. In the peak current mode control approach, the peak current of the inductor is used to force the input current to follow the reference. Despite the simplicity of controlling the input current, this approach presents a low-gain, wide-bandwidth current loop, which generally makes it unsuitable for a high-performance PF corrector, since there is a significant error between the reference and the current. This error will produce distortion and a poor PF.

The conceptual diagram of a CCM boost converter using average current mode control is also shown in Figure 7. This approach is based on a simple concept. The amplifier $G_c(s)$ is used in the feedback loop to average the inductor current. Therefore, the average inductor current is used instead of the peak current to track the reference $i_{ref}(t)$ with very little error. Another important feature of the average current mode control is that near the zero crossings of the line voltage, the converter operates with the maximum duty cycle. As a result, the dead angle period, which is present in the peak current mode control, is reduced. Average current mode control is relatively easy to implement. As a result, it is the method used for the implementation of the active PFC in this experiment.

AC LINE CURRENT HARMONIC STANDARD

International Electrotechnical Commission Standard IEC 61000-3-2

The standard that forms the foundation for both present and proposed future harmonic current standards is the IEC 555 (now the IEC 61000-3-2). The IEC 555 was first released in draft form in 1982, has since received a number of revisions, and is presently considered the de facto worldwide harmonic current emission standard for commercial equipment.

The IEC 61000-3-2 standard covers a number of different types of low-power equipment, with varied harmonic limits. It specifically limits harmonics for equipment having an input current of

up to 16 A, connected to 50 or 60 Hz, 220 V to 240 V single-phase circuits (two or three wires), as well as 380 V to 415 V three-phase (three or four wires) circuits. In a city environment such as a large building, a great fraction of the total power system load can be nonlinear. For example, a major portion of the electrical load in a building is comprised of fluorescent lights, which present a very nonlinear characteristic to the utility system. A modern office may also contain a large number of personal computers, printers, copiers, etc., each of which may employ diode rectifier circuits. Although each individual load is a negligible fraction of the total local load, these loads can collectively become significant.

There are four categories of equipment, each of which is covered by a different limits.

Class A: Consists of balanced three-phase equipment; household appliances, excluding equipment identified as Class D; tools, excluding portable tools; and audio equipment. Equipment not specified in one of the three other classes should be considered to be Class A equipment. These limits are given in Table 1, and are absolute ampere limits.

Table 1. IEC 61000-3-2 harmonic current limits, Class A and certain Class C.

Odd Harmonics		Even Harmonics	
Harmonic Number	Maximum Current	Harmonic Number	Maximum Current
3	2.30 A	2	1.08 A
5	1.14 A	4	0.43 A
7	0.77 A	6	0.30 A
9	0.40 A	$8 \le n < 40$	0.23 A * (8/n)
11	0.33 A		
13	0.21 A		
$15 \le n < 39$	0.15 A * (15/n)		

Class B: Consists of portable tools and arc welding equipment that is not professional equipment. The limits are equal to the Table 1 limits, multiplied by a factor of 1.5.

Class C: Consists of lighting equipment. The input current harmonic of ballasted lamps with an input power of more than 25 W must meet the limits given in Table 2, expressed as a percent of the fundamental current. If the input power is less than 25 W then Table 3 applies. Incandescent lamp fixtures containing phase-control dimmers, rated at greater than 1 kW, must meet the limits

given in Table 1. When testing for compliance, the dimmer must drive a rated-power lamp, with the phase control set to a firing angle of 90° ± 5°. Discharge lamps containing dimmers must meet the limits given in both Tables 2 and 3 at maximum load. Harmonic current at any dimming position may not exceed the maximum load harmonic current.

Table 2. IEC 61000-3-2 harmonic current limits, certain Class C.

Harmonic Number	Maximum Current, Percent of Fundamental
2	2%
3	(30%)*(Power Factor)
5	10%
7	7%
9	5%
$11 \leq n < 39$	3%

Class D: Equipment having a specified power of less than or equal to 1 kW, of the following types: personal computers and personal computer monitors and television receivers. In general, Class D limits are reserved for equipment that can be shown to have a pronounced effect on the public electricity supply system. This pronounced effect could be related to factors such as: number of pieces of equipment in use; duration of use; simultaneity of use; power consumption; and harmonic spectrum, including phase. The limits for Class D equipment are given in Table 3.

The limits given in Table 3 are valid for all applications having an active input power >75 W. No limits apply for equipment with an active input power up to and including 75 W. This lower limit of 75 W will be reduced to 50 W four years after the implementation day of the standard, which will be January 2005.

Table 3. IEC 61000-3-2 harmonic current limits, Class D and certain Class C.

Harmonic Number	Relative Limit (mA/W)	Absolute Limit (A)
3	3.4	2.30 A
5	1.9	1.14 A
7	1.0	0.77 A
9	0.5	0.40 A
11	0.35	0.33

$13 \le n < 39$	$3.85/n$	See Table 1

IEEE/ANSI Standard 519

In 1993, the IEEE published a rewire draft standard limiting the amplitudes of current harmonics, *the IEEE Guide for Harmonic Control and Reactive Compensation of Static Power Converters.* The harmonic limits are based on the ratio of the fundamental component of the load current I_L to the short-circuit current at the point of common coupling (PCC) at the utility I_{sc}. Stricter limits are imposed on larger loads than on smaller ones. The limits are similar in magnitude to the IEC-61000-3-2. Enforcement of this standard is presently up to local utility company.

The odd-harmonic limits are listed in Tables 4 and 5. The limits for even harmonics are 25% of the odd-harmonic limits. DC current components and half-wave rectifiers are not allowed.

Table 4. IEEE-519 maximum odd harmonic current limits for general distribution systems, 120 V through 69 KV.

I_{sc}/I_L	$n < 11$	$11 \le n < 17$	$17 \le n < 23$	$23 \le n < 35$	$35 \le n$	THD
< 20	4.0%	2.0%	1.5%	0.6%	0.3%	5.0%
20 - 50	7.0%	3.5%	2.5%	1.0%	0.5%	8.0%
50 - 100	10.0%	4.5%	4.0%	1.5%	0.7%	12.0%
100 - 1000	12.0%	5.5%	5.0%	2.0%	1.0%	15.0%
> 1000	15.0%	7.0%	6.0%	2.5%	1.4%	20.0%

Table 5. IEEE-519 maximum odd harmonic current limits for general distribution systems, 69.001 KV through 161 KV.

I_{sc}/I_L	$n < 11$	$11 \le n < 17$	$17 \le n < 23$	$23 \le n < 35$	$35 \le n$	THD
< 20	2.0%	1.0%	0.75%	0.3%	0.15%	2.5%
20 - 50	3.5%	1.75%	1.25%	0.5%	0.25%	4.0%
50 - 100	5.0%	2.25%	2.0%	0.75%	0.35%	6.0%
100 - 1000	6.0%	2.75%	2.5%	1.0%	0.5%	7.5%
> 1000	7.5%	3.5%	3.0%	1.25%	0.7%	10.0%

It is the responsibility of the power consumer to meet these current harmonic standards. Standard IEEE-519 also specifies the maximum allowable voltage harmonic, as listed in Table 6. It is the

responsibility of the utility, or power supplier, to meet these limits. Both THD and maximum individual harmonic magnitudes are limited.

Table 6. IEEE-519 voltage distortion limits.

Bus Voltage at PCC	Individual Harmonics	THD
69 KV and Below	3.0%	5.0%
69.0001 KV – 161 KV	1.5%	2.5%
Above 161 KV	1.0%	1.5%

W A R N I N G

Since you will be working with circuits with potentially lethal levels of input and output voltages, you are required to exercise extreme caution to avoid any accidents. Do not touch any part of the circuits (power stage or control) when the circuits are connected to the AC sources and are up and running. Also, be extremely careful when connecting measuring equipment to the circuit. Make all the necessary connections when the AC source is turned off. If you are not sure or you do not know how to use or connect any piece of the equipment, please call a lab instructor. Finally, you are required to wear safety glasses (provided) when running the circuits.

SUGGESTED PROCEDURE

For the realization of this experiment, you are going to use the UCC3817 BiCMOS PF preregulator evaluation board from Texas Instruments. The board schematic is shown in Figure 8. As can be seen, the PF preregulator is based on a CCM boost converter. The main features in the evaluation board are listed as follows:

- Designed to comply with IEC 61000-3-2
- Worldwide line operation RMS voltage range from 85 V to 265 V
- Regulated 385V, 250W (max) DC output
- Accurate power limiting
- Accurate overvoltage protection

The multiplier controller is implemented with the UCC3817 IC chip from Texas Instruments, which simplified the complexity of the control requirements. The controller achieves near-unity PF by shaping the AC input line current waveforms to correspond to that of the AC input line voltage. Average current mode control maintains stable, low-distortion, sinusoidal line current.

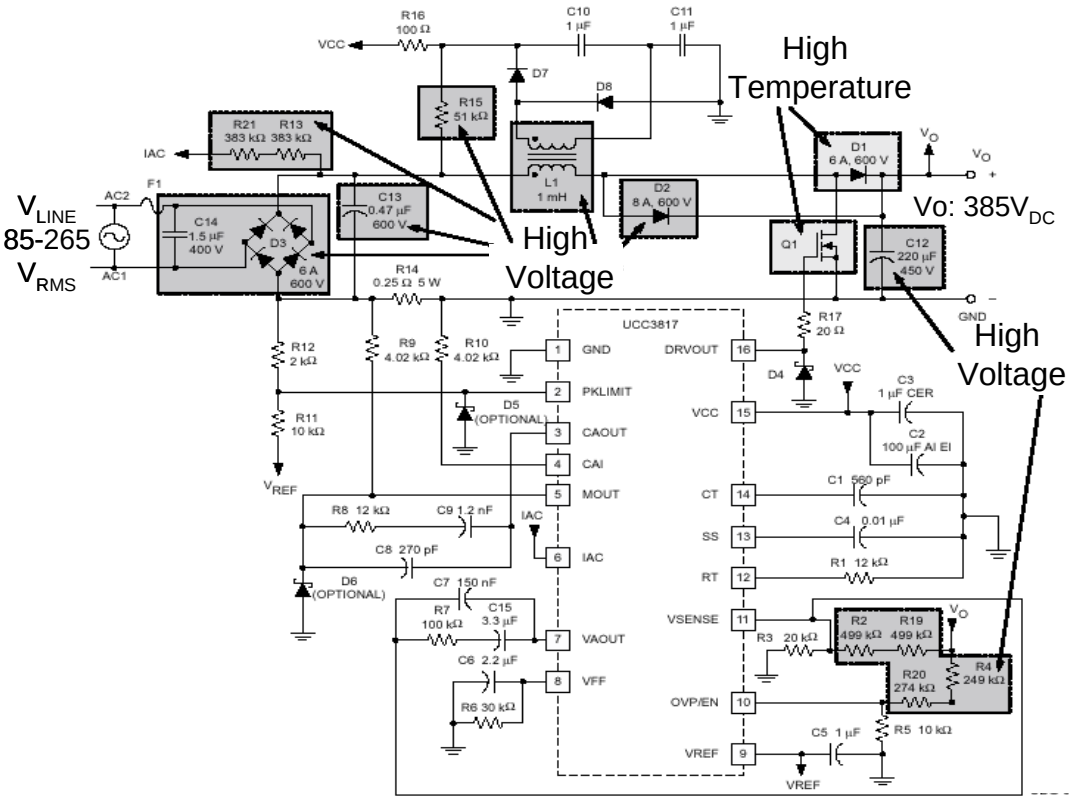


Figure 8. Evaluation board schematic.

Figure 9 shows the evaluation board layout assembly. For safety issues, the high-voltage and high-temperature components are pointed out. At all times, avoid touching these points when the converter is running.

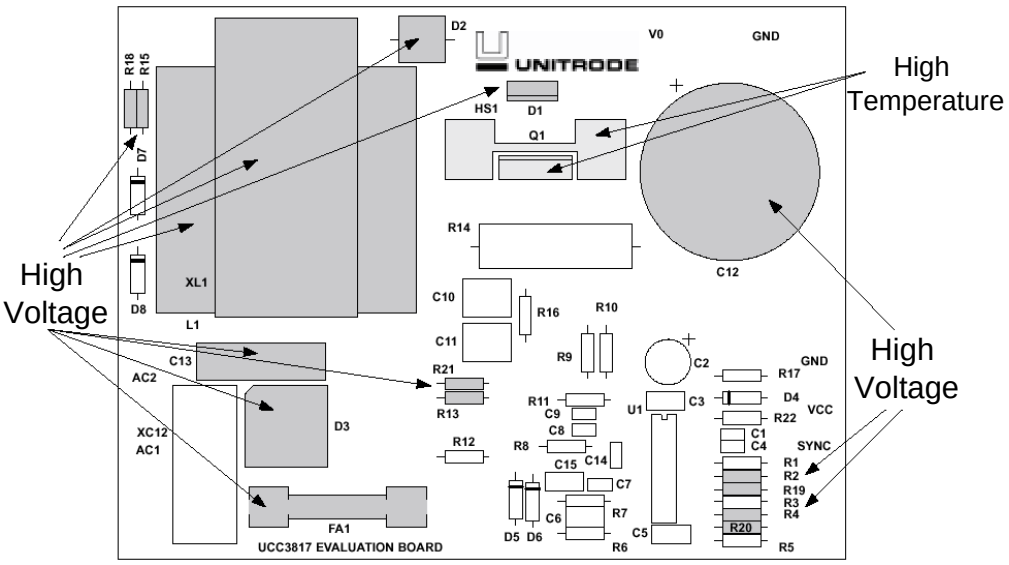


Figure 9. UCC3817 Evaluation board layout assembly.

1. The first part of the experiment consists of measuring the power consumption, the THD and PF of one of the most common pieces of equipment used nowadays: a computer. For this experiment we are going to use the computer that is on top of your bench and a transformer for isolation. To measure the harmonic distortion, it is necessary to connect the DACI to input voltage and the line current shown in Figure 10. With the application function of the DACI, you can measure the fundamental and multiple harmonics. For the power consumption we need to connect a wattmeter (DACI) in the input. The oscilloscope (DACI) is connected so that you can estimate the displacement power factor. Measured from phase angel between the input current (Channel 2) and voltage (Channel 1) measured using the peak locations. After connecting all the equipment, turn on the computer and fill in the table (table1) for power, the individual harmonic for the input current, and the displacement factor for different input voltages.

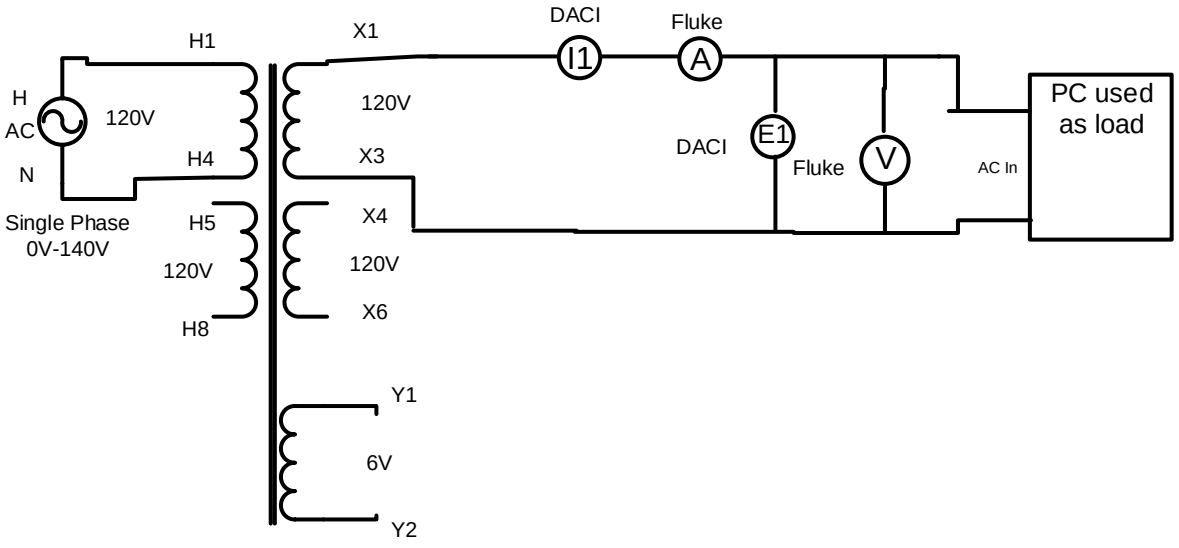


Figure 10. Setup diagram for Part I of the experiment

Vin	Iin	Pin	Pf displacement Estimate from peak location	Pf Total (DACI)	THD (DACI
90Vrms					
100Vrms					
110Vrms					
120Vrms					

Table 1.

2. The second part of the experiment explores the benefits obtained by incorporating a PF stage in the power supply system. For this part, you will use the PF preregulator evaluation board described in the previous paragraphs. In this module, you need to connect a 1000Ω load. Turn all load bank switches to center position the two switches on each load bank down. This will set the load bank to 500Ω use 2 load banks in series in the output, which results in an equivalent load of 148 watts. Similar to Part 1, input Voltage (Chanel 1) line Current (Channel 2) and the wattmeter (DACI) in the input side, as shown in Figure 11. Connect a 3 phase supply using 2 phases. The voltage between 2 of the phases will give us a 85Vrms to 240Vrms line voltage in the input side to adjust the input voltage. Use a transformer for isolation, connect 2 120V primary winding in series and the same for the secondary windings With the variations of the input voltage you can measure the harmonic distortion, PF and the efficiency of the evaluation module for different input voltage conditions. For the efficiency measurement, you need to connect multimeters in the DC output of the evaluation board to measure the power delivered to the load.

   After connecting the equipment, adjust the input voltage to 85 V. At this point the PF corrector should regulate (you will hear a chirp) the output voltage to 385 V. At this instant, you can record the input and output power, the individual fundamental and multiple harmonics of the input current. After that, increase the input voltage in steps and fill in the table (table 2)with the important variables of the circuit. The idea is to construct a curve,

which relates the THD and the PF with variations in the input voltage. It is important to mention that at no time should the input voltage exceed 265 V.

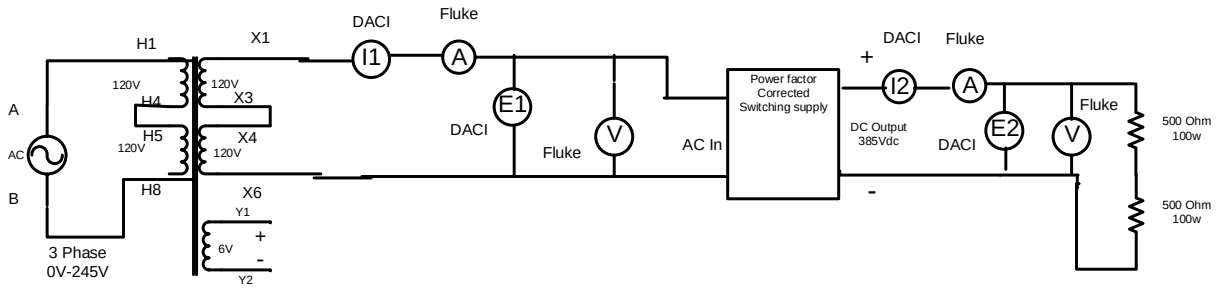


Figure 11. Setup diagram for Part II of the experiment

Vin	Iin	Pin	Pf Displacement	Pf Total (DACI)	Vdc	Idc	Pout DC	Ploss	THD
90Vrms									
120Vrms									
150Vrms									
200Vrms									
220Vrms									

Table 2.