ECE 3274
MOSFET Amplifier Project

1. Objective

This project will show the biasing, gain, frequency response, and impedance properties of the MOSFET common source and common drain amplifiers.

2. Components

Qty	Device
1	2N7000 MOSFET Transistor

3. Introduction

Two of the most popular configurations of small-signal MOSFET amplifiers are the common source and common drain configurations. These two circuits are shown in Figures 1 and 2 respectively. The common source and common drain amplifiers, like all MOSFET amplifiers, have the characteristic of high input impedance. The value of the input impedance for both amplifiers is limited only by the biasing resistors R_{g1} and R_{g2}. Values of R_{g1} and R_{g2} are usually chosen as high as possible to keep the input impedance high. High input impedance is desirable to keep the amplifier from loading the signal source. One popular biasing scheme for the CS and CD configurations consists of the voltage divider R_{g1} and R_{g2}. This voltage divider supplies the MOSFET gate with a constant dc voltage. This is very similar to the BJT biasing arrangement described in common emitter amplifier. The main difference with the BJT biasing scheme is that ideally no current flows from the voltage divider into the MOSFET.

The CS and CD MOSFET amplifiers can be compared to the CE and CC BJT amplifiers respectively. Like the CE amplifier, the CS amplifier has negative voltage gain and output impedance approximately equal to the drain resistor (collector resistor for the CE amplifier). The CD amplifier is comparable to the CC amplifier with the characteristics of high input impedance, low output impedance, and less than unity voltage gain. The corner frequencies of the CS and CD frequency response can also be approximated using the short circuit and open circuit time constant methods.

The 2N7000 MOSFET used in this project are an n-channel enhancement-type MOSFET. For the enhancement-type MOSFET, the gate to source voltage must be positive and no drain current will flow until V_{GS} exceeds the positive threshold voltage V_{TN}. V_{TN} is a parameter of each particular MOSFET and is temperature sensitive. This parameter sensitivity to temperature is one reason for establishing a stable dc bias. The 2N7000 MOSFET data sheet lists the minimum and maximum values of V_{TN} as 0.8 V and 3.0 V respectively.

The MOSFET can be easily damaged by static electricity, so careful handling is important.

You should refer to your lab lecture notes, your Electronics II Lecture notes, your textbook, the course website, and other reference material to determine how best to design your amplifier. This lab is intended as a design project and not as a step-by-step guide.

4. Requirements

Your **common-source** amplifier design must meet the following requirements.

Requirement	Specification
Voltage Gain	$\|A_v\| > 6.0$ V/V
Low Frequency Cutoff	Between 100 Hz and 300 Hz
High Frequency Cutoff	Between 20 kHz and 150 kHz
Input Impedance	Between 5kΩ and 10 kΩ
Output Voltage Swing	Greater than 4.0 V_{pp}
Load Resistance	5.6 kΩ
Power Supply Voltage	12 V_{dc}

Table 1. Common-source amplifier requirements.

Your **common-drain** amplifier design must meet the following requirements.

Requirement	Specification
Voltage Gain	$\|A_v\| > 0.5$ V/V
Low Frequency Cutoff	Between 100 Hz and 300 Hz
High Frequency Cutoff	Between 20 kHz and 150 kHz
Input Impedance	Between 5kΩ and 10 kΩ
Output Voltage Swing	Greater than 6.0 V_{pp}
Load Resistance	220 Ω
Power Supply Voltage	12 V_{dc}

Table 2. Common-drain amplifier requirements.

5. Prelab Design Project

For this project, you will design two distinct amplifiers—the common source and the common drain. These circuits are shown in Figure 1 and 2 respectively. You should refer to your class notes, textbook, instructor, and other reference material to help you design the circuits. Start with the DC design and then move onto the AC design.

Component	Value
R_i	150Ω
For CS Chi2:	100pF
For CD Chi2:	0.022uf
C_{byp}	0.1µF or 0.047uF

Table 3. Fixed component values.

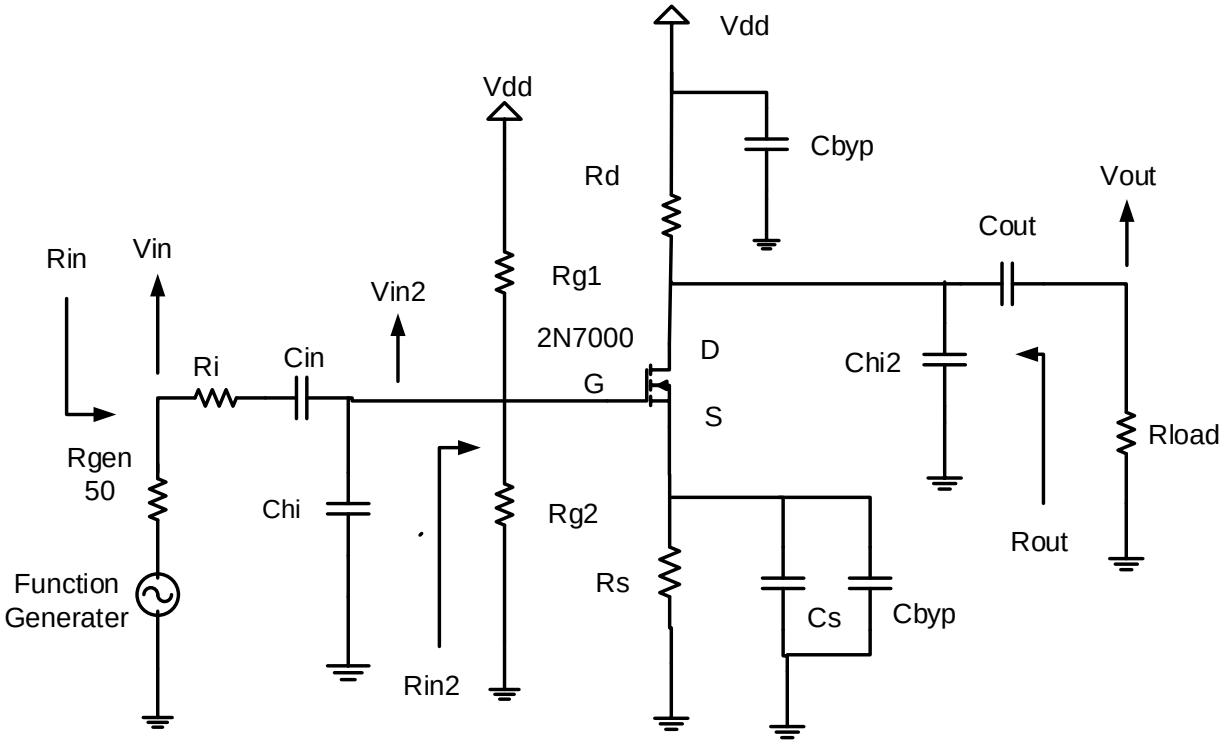

Figure 1. Common-source amplifier circuit.

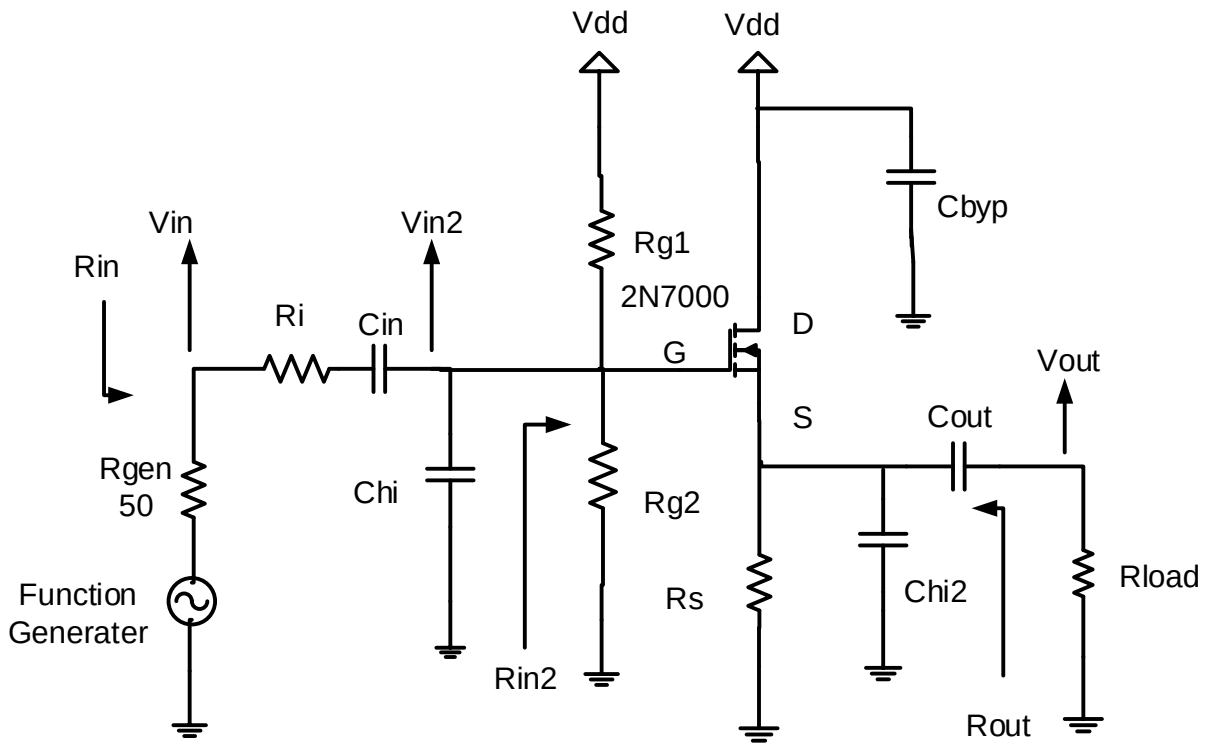

Figure 2. Common-drain amplifier circuit.

5.1 DC Bias

Begin by designing the DC bias networks for the amplifiers. You will start by examining the output requirements to select the Q-point, set Vs to 2V to 3V for the CS amplifier. Once you have designed the DC bias network, use the transistor characteristics for the 2N7000 transistor to determine the transistor parameters from the curves for where you are operating. Note that there is no single correct answer and that your design may differ significantly from your colleagues'. You should show all work and walk through all calculations. You must calculate and show all of the following values for both amplifiers (excluding R_D for the common drain amplifier).

Component Values	Device Parameters	Voltages and Currents
R_{G1}	V_{TN}	V_{DS}
R_{G2}	r_o	V_{GS}
R_S	g_m	V_S
R_D		I_D

Table 3. DC Bias and Amplifier Parameters

5.2 AC Design

Design the ac characteristics of the amplifier. You must calculate and show all of the following values. The high frequency cutoff is controlled by **Chi** = 1/(2 π FH Req). **Chi2** will help prevent high frequency oscillations. Because we will set the all poles for the low frequency break point at the same frequency.

We will use the bandwidth shrinkage formula to adjust the frequency of each pole.

$BWshrinkage = \sqrt{2^{1/n} - 1}$ where (n) number of low frequency pole at the same frequency.

For the CS there are 3 low frequency capacitors Cin, Cout, and Cs so use
FL' = (FL)*(BWshrinkage) where n =3.
Fcin = Fcout = Fcs = FL'
Cin = 1/(2π Fcin Rci) Cout = 1/(2π Fcout Rcout) Cs = 1/(2π Fcs Rcs)

For the CD there are 2 low frequency capacitors Cin, and Cout so use
FL' = (FL)*(BWshrinkage) where n =2.
Fcin = Fcout = FL'
Cin = 1/(2π Fcin Rci) Cout = 1/(2π Fcout Rcout)

Component Values	Amplifier Parameters	Voltages, Currents, and Power
C_{in}	Voltage Gain	v_{in}
C_{out}	Current Gain	v_{out}
C_S (CS only)	Power Gain (in dB)	i_{in}
C_{hi}	Low Frequency Cutoff	i_{out}
	High Frequency Cutoff	p_{in}
	Input Resistance	p_{out}
	Output Resistance	

Table 4. Small Signal (ac) Amplifier Parameters

5.5 Computer-aided Analysis (optional helpful in checking your design)
Once you have completed your two amplifier designs, use LTspice to analyze their performance. You will need to install 2N7000 model for LTspice it is available from the class web site. Generate the following plots:

- **(a)** A time-domain plot of the input and output, with the output voltage of $2.0V_{pk}$ (CS) or $3.0V_{pk}$ (CD) at 5 kHz. The output should not have any distortion or clipping. Calculate the midband gain Remember the gain is Vout/Vin not Vout/Vgen, and indicate it on the plot. Compare this to your calculated values.
- **(b)** An FFT of your time-domain waveform. Circle and indicate the height of any strong harmonics, in dB relative to your fundamental frequency at 5 kHz.
- **(c)** A frequency sweep of the amplifier from 10 Hz to 1 MHz. Indicate the high and low frequencies on the plot (these should correspond to the half-power, or 3dB below midband points). Compare these to your calculated values.

6. Lab Procedure
You must test your 2N7000 MOSFET with the curve tracer before build your experiment.
Set curve trace to N-FET, Is Max = 10ma, Vds max =10V, Vg/step = 0.1V, Offset = 1.8V, Rload=.10, N Steps = 10

6.1. Construct the CS amplifier shown in Figure 1. Remember that R_{gen} is internal to the function generator Fgen = 2kHz. Record the values of the bias network resistors and the capacitors you used in the circuit. R_L = 5.6kΩ

6.2. Measure the following values:
- **(a)** Q-point: V_{GS}, V_{DS}, V_S, V_G, V_D, and I_D (measure voltage across a known resister).
- **(b)** Voltage, current, and power gains.
- **(c)** Maximum undistorted peak-to-peak output voltage.
- **(d)** THD% of output waveform (add distortion step)
- **(e)** Input and output resistance.
- **(f)** Low and high cutoff frequencies and BW (half power point).

Recall that input impedance is given by $R_{in} = v_{in}/i_{in}$ where $I_{in} = V_{Ri} / Ri$, output impedance is given by $R_{out} = (v_{oc}-v_{load})/i_{load}$, voltage gain is given by $A_v = v_{out}/v_{in}$, and current gain is given by $A_i = i_{load}/i_{in}$.

Additionally, plot the following:
- **(a)** Input and output waveform at the maximum undistorted value.
- **(b)** Power spectrum (add step) showing the fundamental and first few harmonics.
- **(c)** Frequency response (ACsweep) from 10 Hz to 1 MHz set the input voltage (generator output) to a value that does not cause distortion across the entire passband of the amplifier.

6.3. Replace the load resistor, RL, with a 560Ω and a 27kΩ resistor, and measure the maximum output swing and voltage gain **without clipping**. Comment on the loading effect, and remember to change back to a 5.6kΩ load resistor after this step.

6.4. Construct the CD amplifier shown in Figure 2. Remember that R_{gen} is internal to the function generator Fgen = 2kHz. Record the values of the bias network resistors and the capacitors you used in the circuit. R_L = 220Ω

6.5. Measure the following values:

(a) Q-point: V_{GS}, V_{DS}, V_S, V_G, V_D, and I_D (measure voltage across a known resister. Assume $I_D = I_S$).

(b) Voltage, current, and power gains.

(c) Maximum undistorted peak-to-peak output voltage.

(d) THD% of output waveform (add distortion step)

(e) Input and output resistance.

(f) Low and high cutoff frequencies and BW (half power or 3dB below midband points).

Recall that input impedance is given by $R_{in} = v_{in}/i_{in}$, output impedance is given by $R_{out} = (v_{oc}-v_{load})/i_{load}$, voltage gain is given by $A_v = v_{out}/v_{in}$, and current gain is given by $A_i = i_{load}/i_{in}$.

Additionally, plot the following:

(a) Input and output waveform at the maximum undistorted value.

(b) Power spectrum (add step) showing the fundamental and first few harmonics.

(c) Frequency response (ACsweep) from 10 Hz to 1 MHz set the input voltage (generator output) to a value that does not cause distortion across the entire passband of the amplifier.

6.6. Replace the load resistor, R_L, with a 100Ω and a 27kΩ resistor, and measure the maximum output swing and voltage gain without output clipping. Comment on the loading effect, and remember to change back to a 220Ω load resistor after this step.

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MOSFET Amplifier Lab
Data Sheet

Name:_____ **Lab Date:**_____ **Bench:**_____

Partner:_____

Remember to include units for all answers and to label all printouts. There are a total of six (8) printouts in this lab. Only one set of printouts is required per group.

You must test your 2N7000 MOSFET with the curve tracer before build your experiment.
Set curve trace to N-FET, Is Max = 10ma, Vds max =10V, Vg/step = 0.1V, Offset = 1.8V, Rload=.10, N Steps = 10

6.1. Common source amplifier component values

R_{G1}:		**R_{G2}:**		**R_D:**		**R_S:**	
C_{in}:		C_{out}:		C_S:		C_{hi}:	
R_L:		Ri:		C_{hi2}:			

6.2. Common-source amplifier. There are 4 printouts (Vin, Vout, Power spectrum, and ACsweep). Fgen = 2kHz.

Q-Point:	V_{GS}:	_____	V_{DS}:	_____	I_D:	_____
	V_S:	_____	V_G:	_____	V_D:	_____
Gain:	Voltage:	_____	Current:	_____	Power:	_____
Voltage Output:	Max:	_____	THD%:	_____		
	Vin:	_____	**V_{Ri}**	_____	**Iin:**	_____
	Vload:	_____	**I_{Load}**	_____	Voc:	_____
Resistance:	Input	_____	Output	_____		
Frequency Response:	Low:	_____	High:	_____	BW	_____

6.3. Common-source amplifier with a variable load resistor. There are no printouts here.
560Ω Resistor:

Gain:	Voltage:	_____	Current:	_____	Power:	_____
Voltage Output:	Max:	_____				

27kΩ Resistor:

Gain:	Voltage:	_____	Current:	_____	Power:	_____
Voltage Output:	Max:	_____				

6.4. Common drain amplifier component values

R_{G1}:		**R_{G2}:**		**R_S:**		**R_L:**		**Ri:**	
C_{in}:		**C_{out}:**		**C_{hi}:**		**C_{hi2}:**			

6.5. Common-drain amplifier. There are 4 printouts (Vin, Vout, Power spectrum, and ACsweep). Assume $I_D = I_S$, Fgen = 2kHz.

Q-Point:	V_{GS}:	_____	V_{DS}:	_____	I_D:	_____
	V_S:	_____	V_G:	_____	V_D:	_____
Gain:	Voltage:	_____	Current:	_____	Power:	_____
Voltage Output:	Max:	_____	THD%:	_____		
	Vin:	_____	V_{Ri}	_____	Iin:	_____
	Vload:	_____	I_{LOAD}	_____	Voc:	_____
Resistance:	Input	_____	Output	_____		
Frequency Response:	Low:	_____	High:	_____	BW	_____

6.3. Common-drain amplifier with a variable load resistor. There are no printouts here.

100Ω Resistor:

Gain:	Voltage:	_____	Current:	_____	Power:	_____
Voltage Output:	Max:	_____				

27kΩ Resistor:

Gain:	Voltage:	_____	Current:	_____	Power:	_____
Voltage Output:	Max:	_____				