ECE 3274
Active Load Common Emitter Amplifier Project

1. Objective

This project will show how the use of an active load in a common emitter amplifier can affect the gain open loop gain.

2. Components

Qty	Device
1	2N2222 NPN Transistor
2	2N3906 PNP Transistor

3. Introduction

This project consists of two amplifier designs. The first amplifier, shown in Figure 2, is a common-emitter amplifier with the emitter grounded and negative feedback provided through R_{b1}, R_{b2} and C_{fdc}. This change serves to stabilize the bias of the amplifier and increase gain. The second amplifier, shown in Figure 3, is a modification of the first with the collector resistor replaced with a current mirror. This has the effect of increasing the open loop gain of the amplifier significantly. Figure 1 shows the customary front-end filter, which is required for both amplifiers and replaces R_s' in each schematic.

R_{b1} and R_{b2} with C_{fdc} to form the DC negative feedback path. R_{b1}, R_{b2}, and R_{b3}, with Vce, form the voltage divider to bias the transistor Q-point. This is needed because we did not use an emitter resistor to control I_c and provide negative feedback in the DC bias circuit. The selection of the C_{fdc} needs to such that the high frequency cutoff of the feedback network is below the amplifier low frequency cutoff. Set $R_{b1} = R_{b2}$ in your design and set the current through R_{b1} and R_{b2} to at ten times the base current. Set the current though R_{b3} to nine times the base current.

For the AC design, assume that the midpoint of the feedback network is a ground at the midband frequency. This means that R_{b2} is in the input impedance design and R_{b1} is in the output impedance design.

For the active load design, set $R_{e2} = R_{e3}$ and set the voltage across the resistors to 1V.

You should refer to your lab lecture notes, your Electronics II Lecture notes, your textbook, the course website, and other reference material to determine how best to design your amplifier. This lab is intended as a design project and not as a step-by-step guide.

4. Requirements
Both amplifier designs must meet the following requirements.

Requirement	Specification
Collector Current Q1	3mA
Low Frequency Cutoff	Between 100 Hz and 300 Hz
Hi Frequency Cutoff	Between 50 kHz and 150 kHz
Base Resistors	$R_{b1} = R_{b2}$
Output Voltage Swing	Greater than 4.0 V_{pk-pk}
Load Resistance	1.5 kΩ
Power Supply Voltage	9 V_{dc}

Table 1. Amplifier requirements.

Use the same base resistor values for both amplifiers, and maintain the same collector-emitter voltage (in other words, the Q-point for both amplifier designs should be the same).

5. Prelab Design Project
For this project, you will design two amplifiers—a common-emitter amplifier without and with an active load. These circuits are shown in Figure 2 and 3 respectively. You should refer to your class notes, textbook, instructor, and other reference material to help you design the circuits. Start with the DC design and then move onto the AC design. Use the following fixed component values in your circuit:

Component	Value
R_i	150Ω
C_{byp}	0.1µF
C_{fdc}	47µF
Q1 r_o	60kΩ
Q2,Q3 r_o	30kΩ
V_{BE}	0.65V
β	150

Table 2. Fixed component values.

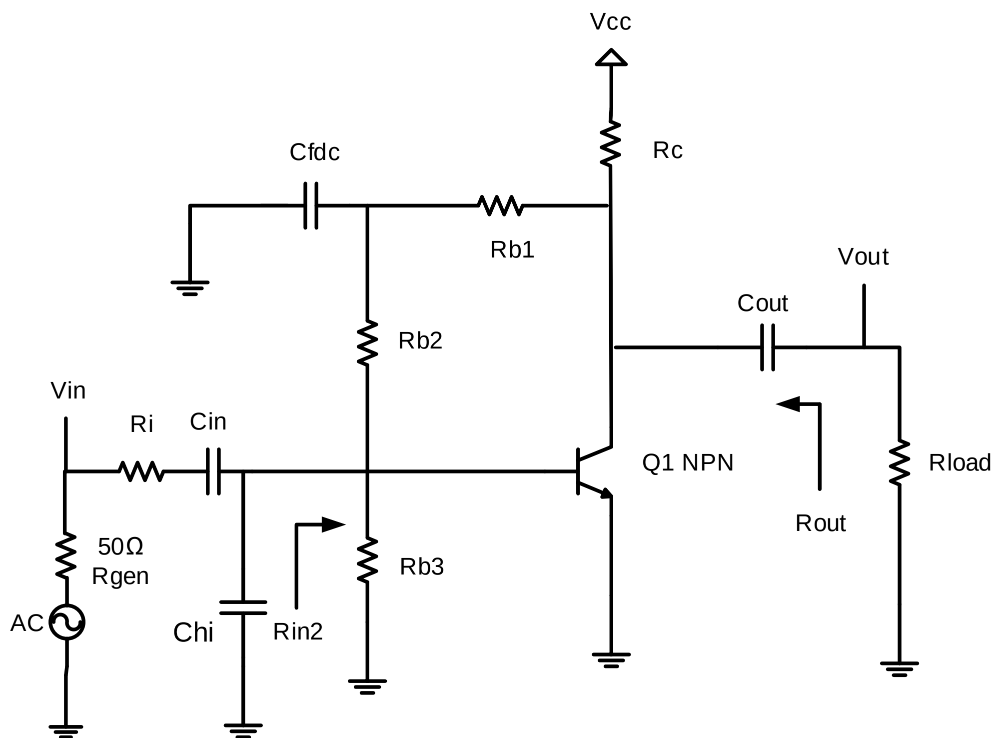

Figure 1. Common-emitter amplifier without active load.

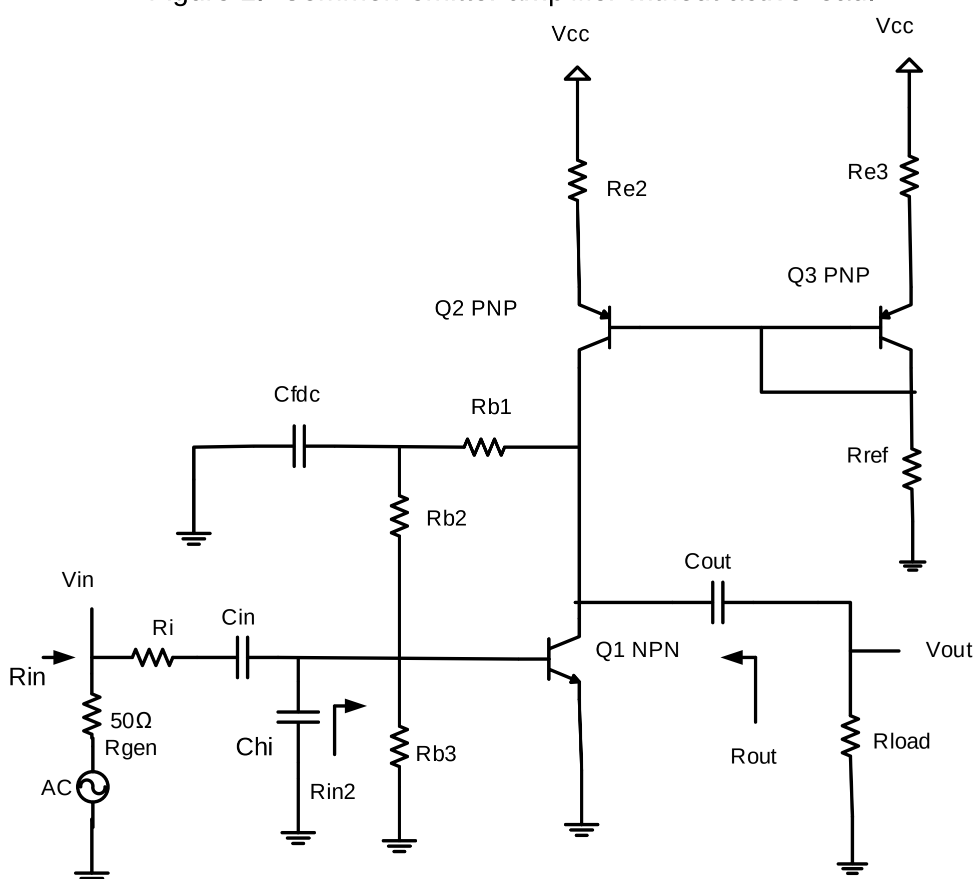

Figure 2. Common-emitter amplifier with active load.

5.1 DC Bias (35 point)
Begin by designing the DC bias networks for the amplifiers. Once you have designed the DC bias network, use the transistor characteristics for the 2N2222 and 2N3906 (second design, for current mirror) transistors to determine the transistor parameters for where you are operating. Note that there is no single correct answer and that your design may differ significantly from your colleagues. You should show all work and walk through all calculations. You must calculate and show all of the following values for both amplifiers (excluding R_{e2}, R_{e3} and R_{ref} for the first design).

Component Values	Device Parameters	Voltages and Currents
R_{b1} – R_{b3}	Beta dc	V_{ce}
R_c	Beta ac	V_{be}
R_{e2} and R_{e3}	r_π	V_e
	r_o	I_c
		I_b

Table 3. DC Bias and Amplifier Parameters

5.2 AC Design (35 point)
Design the ac characteristics of the amplifier. You must calculate and show all of the following values. We will set the poles for the low frequency break point at the same frequency. The Cfdc has a break point below Cin and Cout so we will ingnore it.

$BWshrinkage = \sqrt{2^{1/n} - 1}$ where (n = 2) number of low frequency pole at the same frequency.
$F_L = (F_{Cin} + F_{Cout}) / (BWshrinkage * n)$.
We need adjust the frequency because of bandwidth shrinkage.
Set Fcin =Fcout = F_L*(BWshrinkage)
Cin = 1/(2π Fcin Rci) Cout = 1/(2π Fcout Rcout)

Component Values	Amplifier Parameters	Voltages, Currents, and Power
C_{in}	Voltage Gain	v_{in}
C_{out}	Current Gain	v_{out}
	Power Gain (in dB)	i_{in}
	Low Frequency Cutoff	i_{out}
	High Frequency Cutoff	p_{in}
	Input Resistance	p_{out}
	Output Resistance	

Table 4. Small Signal (ac) Amplifier Parameters

5.5 Computer-aided Analysis Spice (Required) (30 point)
Once you have completed your two amplifier designs, use LTspice to analyze their performance. Generate the following plots:

- **(a)** A time-domain plot of the input and output, with the output voltage of 2.0V_{pk} at 20 kHz. The output should not have any distortion or clipping. Calculate the midband gain and indicate it on the plot. Compare this to your calculated values.
- **(b)** An FFT of your time-domain waveform. Circle and indicate the height of any strong harmonics, in dB relative to your fundamental frequency at 20 kHz.
- **(c)** A frequency sweep of the amplifier from 10 Hz to 1 MHz. Indicate the high and low frequencies on the plot (these should correspond to the half-power, or 3dB below midband points). Compare these to your calculated values.

6. Lab Procedure

6.1. Construct the CE amplifier shown in Figure 1. Remember that the 50Ω resistor is internal to the function generator and is not in your circuit. Record the values of the bias network resistors and the capacitors you used in the circuit. Remember to add the front end circuit.

6.2. Measure the following values:

- **(a)** Q-point: V_{CE}, V_{BE}, V_E, I_C and V_{E2}.
- **(b)** Voltage, current, and power gains.
- **(c)** Maximum undistorted peak-to-peak output voltage.
- **(d)** Input and output resistance.
- **(e)** Low and high cutoff frequencies (half power point).

Recall that input impedance is given by $R_{in} = v_{in}/i_{in}$, output impedance is given by $R_{out} = (v_{oc}-v_{load})/i_{out}$, voltage gain is given by $A_v = v_{out}/v_{in}$, and current gain is given by $A_i = i_{out}/i_{in}$.

Additionally, plot the following:

- **(a)** Input waveform (adjust input for undistorted output) and output waveform at the maximum undistorted value.
- **(b)** Power spectrum showing the fundamental at 20 kHz and first few harmonics. Add a step to scope capture (Analysis –Frequency domain measurements – Power spectrum).
- **(c)** Frequency response from 10 Hz to 1 MHz (set the input voltage to a value that does not cause distortion across the entire passband of the amplifier).

6.3. Construct the CE with active load amplifier shown in Figure 2. Remember that the 50Ω resistor is internal to the function generator and is not in your circuit. Record the values of the bias network resistors and the capacitors you used in the circuit.

6.4. Repeat section 6.2 for this design.

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Data Sheet

Name:____________________ **Lab Date:**_____________ **Bench:**____________

Partner:____________________

Remember to include units for all answers and to label all printouts. There are a total of six (8) printouts in this lab. Only one set of printouts is required per group.

6.1. Component values for common-emitter amplifier.

R_{b1}: ________ **R_{b2}:** ________ **R_{b3}:** ________
R_c: ________ **R_L:** ________

6.2. Common-emitter amplifier. There are 4 plots (Vin, Vout, Power spectrum, and ACsweep).

Capacitor Values:	C_{in}:	________	C_{out}:	________	C_{fdc}:	________
Q-Point:	V_{CE1}:	________	V_{BE1}:	________	V_{E1}:	________
	I_{C1}:	________		________		
Gain:	Voltage:	________	Current:	________	Power:	________
Voltage Output:	Max:	________				
	Vin	________	**V_{Ri}**	________	**Voc**	________
	Iin	________	I_{Load}	________	V_{Load}:	________
Resistance:	Input	________	Output	________		
Frequency Response:	Low:	________	High:	________		

6.3. Component values for common-emitter amplifier with **active load** amplifier.

R_{b1}: ________ **R_{b2}:** ________ **R_{b3}:** ________ **R_{ref}:** ________
R_{e2}: ________ **R_{e3}:** ________ **R_L:** ________

6.4. Common-emitter amplifier with active load. There are 4 plots (Vin, Vout, Power spectrum, and ACsweep).

Capacitor Values:	C_{in}:	________	C_{out}:	________	C_{fdc}:	________
Q-Point:	V_{CE1}:	________	V_{BE1}:	________	V_{E1}:	________
	I_{E2}:	________	I_{ref}:	________	V_{E2}:	________
Gain:	Voltage:	________	Current:	________	Power:	________
Voltage Output :	Max:	________				
	Vin	________	V_{Ri}	________	Voc	________
	Iin	________	I_{Load}	________	V_{Load}:	________
Resistance:	Input	________	Output	________		
Frequency Response:	Low:	________	High:	________		